(54) Title: DIGITAL DISCRETE-TIME NON-FOSTER CIRCUITS AND ELEMENTS

![FIGURE 1](image-url)

(57) Abstract: A method to implement circuits and circuit elements having one or more ports may include digitizing, using analog-to-digital converters, continuous-time input signals received from one or more ports of a circuit to form discrete-time input signals. At a digital signal processor, the discrete-time input signals are received and the discrete-time input signals are processed to calculate a desired discrete-time output signals. Using digital-to-analog converters, the calculated desired discrete-time output signal are calculated to form outputs of continuous-time output signals at the one or more ports of the circuit. The continuous-time output signals are output to the same one or more ports that receive the continuous-time input signals; and producing, thereby, a desired relationship between the continuous-time output signals and the continuous-time input signals at the one or more ports.
DIGITAL DISCRETE-TIME NON-FOSTER CIRCUITS AND ELEMENTS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority to U.S. Provisional Application No. 61/984,377, filed on April 25, 2014, and to U.S. Provisional Application No. 62/061,441, filed on October 8, 2014, both of which are incorporated herein in their entireties.

STATEMENT ABOUT FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] This invention was made with Government support under award number ECCS-1101939 by the National Science Foundation. The Government has certain rights in the invention.

BACKGROUND

[0003] Non-Foster circuits and non-Foster circuit elements are of particular interest in electromagnetics, metamaterials, and antenna applications. Such circuits are useful to increase bandwidth of systems and to perform functions not possible in naturally-occurring circuits and devices. However, non-Foster circuits are heretofore only available using analog circuits and may have some concomitant shortcomings, including not being stable.

SUMMARY OF INVENTION

[0004] Embodiments of the present application pertain to the use of signal processing and discrete-time methods and circuits to implement non-Foster elements and non-Foster circuits having one or more ports, and with options for adaptive control of the circuits.

[0005] According to one aspect, provided herein are digital discrete-time implementations of non-Foster circuits, such as negative capacitors and negative inductors. According to another aspect, adaptive controllers may be employed to stabilize non-Foster circuits and adapt to variations in externally-connected circuits. According to another aspect, two-port or multi-port discrete-time implementations of non-Foster circuits may be employed. According to another aspect, a voltage is measured at one port and the current at the very same port is forced to be a desired value, as determined by digital signal processing. According to another aspect, a current is measured at one port and the voltage at the very same port is forced to be a desired value, as determined by digital signal processing.

[0006] According to one embodiment, a method to implement circuits and circuit elements having one or more ports may include digitizing, using analog-to-digital converters, continuous-time input signals received from one or more ports of a circuit to form discrete-time input signals. At a digital signal processor, the discrete-time input signals are received and the discrete-time input signals are processed to calculate a desired discrete-time output signals. Using digital-to-analog converters, the calculated desired discrete-time output signal are calculated to form outputs of continuous-time output signals at the one or more ports of the circuit. The continuous-time output signals are output to the same one or more ports that receive the continuous-time input signals; and producing, thereby, a desired relationship between the continuous-time output signals and the continuous-time input signals at the one or more ports.

[0007] According to another embodiment, an apparatus to implement circuits and circuit elements having one or more ports may include: analog-to-digital converters at every port to convert continuous-time input signals
received from each port of a circuit into corresponding discrete-time input signals; a digital signal processor to process and compute desired discrete-time output signals for each port from the said discrete-time input signals; digital-to-analog converters at each port to convert the desired discrete-time output signals to continuous-time output signals at each port; and outputs of said digital-to-analog converters connected to the inputs of said analog-to-digital converters at every port. The continuous time output signals may be currents when said continuous-time input signals are voltages, and the continuous time output signals may be voltages when said continuous-time input signals are currents.

**BRIEF DESCRIPTION OF DRAWINGS**

[0008] Aspects of the present invention are further described in the detailed description which follows in reference to the noted plurality of drawings by way of non-limiting examples of embodiments of the present invention in which like reference numerals represent similar parts throughout the several views of the drawings and wherein:

[0009] Figure 1 shows a diagrammatic illustration of a non-Foster element according to an embodiment.

[0010] Figure 2 shows a diagrammatic illustration of a non-Foster element according to an embodiment.

[0011] Figure 3 shows a diagrammatic illustration and simulation of a circuit having at least one non-Foster element according to an embodiment.

[0012] Figure 4 shows a graph of a time-domain simulation of the circuits of Figures 1 and 3 according to one embodiment.

[0013] Figure 5 shows a graph of real and imaginary port impedance for a large-signal s-parameter simulation of the circuit of Figures 1 and 3 according to one embodiment.

[0014] Figure 6 shows a graph of real and imaginary port impedance for a large-signal s-parameter simulation of the circuit of Figures 1 and 3 according to another embodiment.

[0015] Figure 7 shows a diagrammatic illustration and simulation of a circuit having at least one non-Foster element according to an embodiment.

[0016] Figure 8 shows a graph of real and imaginary port impedance for a large-signal s-parameter simulation of the circuit of Figures 1 and 7 according to one embodiment.

[0017] Figure 9 shows a diagrammatic illustration of a non-Foster element according to Figure 2 in accordance with an embodiment.

[0018] Figure 10 shows a graph of real and imaginary port impedance for a large-signal s-parameter simulation of the circuit of Figures 2 and 9 according to one embodiment.

[0019] Figure 11 shows a diagrammatic illustration and simulation of a circuit having at least one non-Foster element with the configuration of Figure 2 according to an embodiment.

[0020] Figure 12 shows a graph of real and imaginary port impedance for a large-signal s-parameter simulation of the circuit of Figures 2 and 11 according to one embodiment.

[0021] Figure 13 shows a diagrammatic illustration of a non-Foster element with adaptive control according to an embodiment.
[0022] Figure 14 shows a diagrammatic illustration of non-Foster circuit having two ports according to an embodiment.

[0023] Figure 15 shows a diagrammatic illustration of non-Foster circuit having two ports according to another embodiment.

[0024] Figure 16 shows a diagrammatic illustration and simulation of a circuit having at least one non-Foster element with the configuration of Figure 14 according to an embodiment.

[0025] Figure 17 shows a graph of real and imaginary port impedance for a large-signal s-parameter simulation of the circuit of Figure 14 according to one embodiment.

[0026] Figure 18 shows a diagrammatic illustration of a non-Foster element according to another embodiment.

[0027] Figure 19 shows a diagrammatic illustration of a non-Foster element according to another embodiment.

[0028] Figure 20 illustrates a flowchart of a method of operation of a non-Foster circuit according to an embodiment.

[0029] Figure 21 illustrates a flowchart of a method of operation of a non-Foster circuit of Figure 1 according to another embodiment.

[0030] Figure 22 illustrates a flowchart of a method of operation of a non-Foster circuit of Figure 2 according to another embodiment.

[0031] Figure 23 illustrates a flowchart of a method of operation of a non-Foster circuit of Figure 14 according to another embodiment.

**DETAILED DESCRIPTION**

[0032] Non-Foster circuit elements and non-Foster circuits, as described herein, may be used in a variety of applications such as magnetic conductors, wideband antennas, metamaterials, and bandwidth enhancement of many circuits. Non-Foster circuit elements could include devices such as negative capacitors, negative inductors, and negative resistors. In prior art, non-Foster circuits may employ negative impedance converters (NIC) and negative impedance inverters (NII) comprised of a variety of continuous-time analog current conveyor circuits or continuous-time analog transistor circuits. Embodiments described herein may pertain to the use of digital signal processing and discrete-time methods and circuits to implement non-Foster elements and non-Foster circuits having one or more ports (e.g., connection points, etc.), and with options for adaptive control of the circuits. The digital signal processing and discrete-time approach offers significant advantages such as low cost, repeatability, scalability, and ease of incorporation of adaptive control methods and adaptive stabilization methods. Digital signal processing is commonly carried out using logic circuits and microcontrollers, but discrete-time signal processing may also be implemented in analog hardware, in delay lines, in analog signal samplers, in digital circuits, in software, or in combinations of these means. Digital discrete-time implementations of non-Foster circuits, such as negative capacitors and negative inductors are described herein as one aspect of the present application. Adaptive controllers to stabilize non-Foster circuits are also described herein as another aspect of the present application. Adaptive controllers to adapt non-Foster circuits to variations in external circuits are also described herein as another aspect of the present application. Discrete-time implementations of
non-Foster circuits having two or more ports are also described herein as another aspect of the present application. A variety of embodiments are presented to illustrate the invention, but it should be understood that these embodiments are merely illustrative, and the present invention is not intended to be limited to these exemplary embodiments.

[0033] In a first embodiment illustrated in Figure 1, an analog continuous-time input voltage v(t) with Laplace transform V(s) is converted to a digital discrete-time signal v[n] by an analog-to-digital voltage converter (ADCv) with clock period T, processed digitally with a discrete-time system having impulse response h[n] with z-transform H(z) (e.g., an example of a digital signal processor (DSP)) having output discrete-time signal l[n]=v[n]*h[n] (with * denoting convolution), so l(z)=H(z)V(z), and finally discrete-time signal l[n] is converted to an analog continuous-time output current i(t) (e.g., an example of a desired current at the port of the non-Foster circuit/element) with Laplace transform I(s) by a digital-to-analog current converter (DACi) with clock period T. It should be understood that signals may be chosen to be single-ended or differential in implementation. For this embodiment:

[0034] I(s)=V*(s) \{ H(z)(1 - z^-1)/s \} z=exp(-sT) = \sum V(s - j2m\pi/T)/T \{ H(z)(1 - z^-1)/s \} z=exp(-sT) for integer m, and where the starred transform is V*(s) = \sum V(nT)e^{-nsT} for integer n.

[0035] For samples sliced without aliasing, the input impedance below the Nyquist frequency becomes:

[0036] Z(s) = V(s)/I(s) = \{ s T/([1 - z^-1])H(z) \} z=exp(-sT) = s T[H(e^{-sT})(1 - e^{-sT})], for frequencies below 0.5/T Hz, assuming a zero-order hold (ZOH) incorporated into the DACi, and where the continuous-time frequency response at low frequencies can be approximated as H(\omega)=H(z)|z=exp(j\omega T). In this embodiment, an example of digital signal processing defined through H(z) is now given for a negative or positive capacitance. Since a capacitor has i(t) = C dv(t)/dt and l(s) = s C V(s), a positive or negative capacitor may be approximated by using the discrete-time backward-difference approximation of the derivative dv(t)/dt \approx (v[n] - v[n-1])/T and setting i[n] = C (v[n] - v[n-1])/T, or equivalently setting i(z) = C (1 - z^-1)V(z)/T. Since I(z)=H(z)V(z) in Fig. 1, H(z) = C (1 - z^-1)/T, thus establishing the necessary digital signal processing. Alternatively, a positive or negative capacitor may be approximated by using the bilinear transform of l(s) = s C V(s), replacing s by 2(z-1)/(\{z+1\}T) yielding I(z) = 2C V(z) (z - 1)/(\{z + 1\} T), so H(z)=2C (z - 1)/(\{z + 1\}T) in Fig. 1, thus establishing an alternative digital signal processing. Similarly in this embodiment, since an inductor has i(t) = i(0) + \int v(t)dt and I(s) = V(s)/(s L), a positive or negative inductor may be approximated by using the discrete-time accumulator approximation to integral i(0) + \int v(t)dt/L \approx i(0) + \sum v[n] T/L, and setting i[n] = i[n-1] + T v[n]/L, or equivalently setting I(z) = T V(z)/(L - z^-1)S, so H(z)=T/L - z^-1S in Fig. 1. Alternatively, a positive or negative inductor may be approximated by using the bilinear transform approximation of the relation I(s) = V(s)/(s L), replacing s by 2(z-1)/(\{z+1\}T) and yielding I(z) = T V(z) (z + 1)/(\{2 L (z - 1)\}), so H(z)= T(z + 1)/(\{2 L (z - 1)\}) in Fig. 1. It should be understood that any Foster or non-Foster impedance Z(s) may be approximated by appropriate selection of discrete-time signal processing system H(z) or h[n], where such discrete-time signal processing may be accomplished in hardware, software, or combination of hardware and software. As illustrated in Fig. 1 and the foregoing example, preferentially the ADCv would have high input impedance and DACi would have high output.
impedance, for simplicity in exposition, such that the current into the ADCv would be approximately zero and the port current approximately equal to the DACi output current.

In a second embodiment illustrated in Figure 2, an analog continuous-time input current \( i(t) \) with Laplace transform \( I(s) \) is converted to a digital discrete-time signal \( i[n] \) by an analog-to-digital current converter (ADCI) with clock period \( T \), processed digitally with a discrete-time system having impulse response \( h[n] \) and \( z \)-transform \( H(z) \) (e.g., a DSP), having output discrete-time signal \( v[n] = [i[n]*h[n]] \) (with \( * \) denoting convolution), so \( V(z) = H(z)I(z) \), and finally discrete-time signal \( v[n] \) is converted to an analog continuous-time output voltage \( v(t) \) with Laplace transform \( V(s) \) by a digital-to-analog voltage converter (DACv) with clock period \( T \). It should be understood that signals may be chosen to be single-ended or differential in implementation. For this embodiment,

\[
\begin{align*}
V(s) &= \mathcal{I}^*(s) \{ \frac{H(z)(1 - z^{-1})}{s} \} = \sum \{ (s - j2\pi n T)/T \} \{ \frac{H(z)(1 - z^{-1})}{s} \} = \sum \{ e^{-sT} \}^m \text{ for integer } m, \\
\text{and where starred transform } \mathcal{I}^*(s) &= \sum \{ nT e^{-sT} \} \text{ for integer } n. \\
\text{For signals sampled without aliasing, the input impedance below the Nyquist frequency becomes: }
\end{align*}
\]

\[
Z(s) = \frac{V(s)}{I(s)}(1 - z^{-1})/(s T) = H(e^{sT})(1 - e^{-sT})/(s T),
\]

for frequencies below 0.5/T Hz, assuming a zero-order hold (ZOH) incorporated into the DACv, and where the continuous-time frequency response at low frequencies can be approximated as \( H(\omega) = H(z) \mid z = \exp(sT) \).

In this embodiment, since an inductor has \( v(t) = L (di/dt) \) and \( V(s) = L \mathcal{I}(s) \), a positive or negative inductor may be approximated by using the discrete-time backward-difference approximation of the derivative \((di/dt) \approx (i[n] - i[n-1])/T\) and setting \( v[n] = L ((i[n] - i[n-1])/T, \) or equivalently setting \( V(z) = L(1 - z^{-1})I(z)/T. \) Since \( V(z) = H(z)I(z) \) in Fig. 2, \( H(z) = L(1 - z^{-1})/T. \) Alternatively, a positive or negative inductor may be approximated by using the bilinear transform \( V(s) = L \mathcal{I}(s) \), replacing \( s \) by \( 2(z - 1)/(z + 1) \) yielding \( V(z) = 2L \mathcal{I}(z) (z - 1)/(z + 1) \), so \( H(z) = 2L(1 - 1)/(z + 1) \) in Fig. 2. Similarly in this embodiment, since a capacitor has \( v(t) = v(0) + \int_0^t \mathcal{I}(t)dt/C \) and \( V(s) = \mathcal{I}(s)/s(C) \), a positive or negative capacitor may be approximated by using the discrete-time accumulator approximation to the integral \( v(0) + \int_0^t \mathcal{I}(t)dt/C \approx v(0) + \sum \{ i[n] T/C, \) and setting \( v[n] = [v[n-1] + T \mathcal{I}(n)/C, \) or equivalently setting \( V(z) = T \mathcal{I}(z)/(C - z^{-1}C), \) so \( H(z) = T/(C - z^{-1}C) \) in Fig. 2. Alternatively, a positive or negative capacitor may be approximated by using the bilinear transform of the relation \( V(s) = \mathcal{I}(s)(s/C, \) replacing \( s \) by \( 2(z - 1)/(z + 1) \) and yielding \( V(z) = T \mathcal{I}(z)(z + 1)/[2 C (z - 1)], \) so \( H(z) = T (z + 1)/[2 C (z - 1)] \) in Fig. 2. It should be understood that any Foster or non-Foster impedance \( Z(s) \) may be approximated by appropriate selection of discrete-time signal processing system \( H(z) \) or \( h[n], \) where such discrete-time signal processing may be accomplished in hardware, software, or combination of hardware and software. As illustrated in Fig. 2 and the foregoing example, preferentially the ADCi would have low input impedance and DACv would have low differential output impedance, for simplicity in exposition, such that the voltage drop across the ADCi would be approximately zero and the port voltage approximately equal to the DACv output voltage.

It should be understood in the embodiments of Fig. 1 and Fig. 2 that a zero-order hold may be replaced by first-order hold, fractional-order hold, perfect reconstruction filters, and the like. It should be understood that the linear time-invariant system \( H(z) \) with impulse response \( h[n] \) in the embodiments of Fig. 1 and Fig. 2 may be replaced by nonlinear systems, time invariant systems, and other general-purpose systems to achieve the
desired relationship of \(i(t)\) and \(v(t)\) at the input port. It should be understood that the embodiments of Fig. 1 and Fig. 2 may be used to implement circuits that satisfy Foster's theorem, in addition to non-Foster circuits.

**[0042]** Fig. 3 is a Keysight ADS simulation schematic of the configuration of Fig. 1, with delay lines, sampler switch, and hold capacitor C1 used to simulate sampling at 1 GHz, \(T=1\) ns, with \(\ln = C(v[n] - v[n-1])/T = -0.005(v[n] - v[n-1]),\) so design value is \(C = 0.005\) T = -5 pF. This simulation schematic is discussed in more detail below.

**[0043]** An example negative capacitance implementation of the configuration of Fig. 1 is illustrated in the Keysight ADS schematic of Fig. 3. The Keysight ADS software offers large signal s-parameters for microwave impedance measurement, but does not appear to have convenient means for mixed-signal simulation; therefore, the ADCv of Fig. 1 is implemented as switch V1 and hold capacitor C1 in Fig. 3, the unit delay is simulated by 1 ns delay line TLD1, the discrete-time subtraction \(v[n] - v[n-1]\) is performed by voltage-controlled voltage source SRC3, and finally the DACI is implemented with voltage-controlled current source SRC4 having transconductance 0.005 S. SRC6, SRC7, and SRC10 are unity-gain voltage buffers, and the input of delay line TLD1 corresponds to \(v[n]\) and output of TLD1 corresponds to \(v[n-1]\). The switch V1 and hold capacitor C1 are used under control of clock oscillator SRC5 to sample at 1 GHz, and \(T=1\) ns. From the foregoing theory for a capacitance C, \(\ln = C(v[n] - v[n-1])/T\) and in the circuit of Fig. 3, \(\ln = -0.005(v[n] - v[n-1]),\) resulting a design value of \(C = -0.005\) T = -5 pF. The Keysight ADS time-domain simulation of the circuit of Fig. 3 is shown in Fig. 4, with red dotted input voltage \(v(t)\) at 100 MHz, green solid sampled input voltage \(v[n]\), and blue dashed input current \(i(t)\) in mA. From the peak input current of 4.4 mA and peak input voltage of 1.5 V, the magnitude of the impedance is approximately 341 ohms at the 100 MHz signal frequency, versus a predicted impedance of +j318 ohms for -5 pF. Finally, Fig. 5 shows a Keysight ADS large-signal s-parameter simulation of the configuration of Fig. 1 and schematic of Fig. 3, with \(T=1\) ns and C = -5 pF. The dashed red curve is the real part of the input impedance \(Z(s)\), and the solid blue curve is the imaginary part of the input impedance \(Z(s)\). The predicted impedance is approximately +j318 ohms for -5 pF at 100 MHz, and the observed impedance of -182 + j282 ohms at 100 MHz, corresponds to 5.6 pF in series with -182 ohms, versus a predicted impedance of +j318 and -5 pF. The resistive part of the impedance is partially due to the phase contribution of the zero order hold in the implementation. It should be understood that the zero-order hold contributes a time delay of approximately one half clock period, or 0.5 ns in Fig. 3, corresponding to a phase lag of \(2\pi(0.5)/10 = 0.31\) rad or 18 degrees in \(i(t)\). For small angles the effect of phase lag can be estimated as \(+j318/e^{0.31} = -97 + j303\) ohms. A better predicted value of parasitic resistance can be calculated from the relation \(Z(s) = [s T/(1 - z^{-1})]H(z)]_{z=e^{j\omega T}} = [s T/(1 - z^{-1}) C(1 - z^{-1})/T]_{z=e^{j\omega T}} = -193 + j266,\) and is in good agreement with the simulation results of \(-182 + j282\) ohms at 100 MHz. In addition, the shape of the reactance (solid blue curve) in Fig. 5 follows the expected inverse frequency dependence of \(\text{Im}(Z(j\omega)) = +1/(\omega C)\) for a negative capacitor.

**[0044]** As mentioned above, Fig. 4 illustrates a Keysight ADS time-domain simulation of the configuration of Fig. 1 and schematic of Fig. 3, with \(T=1\) ns and C = -5 pF, and predicted impedance of +j318 ohms. The dotted line is input voltage \(v(t)\), solid curve is sampled input voltage \(v[n]\), and dashed line is input current \(i(t)\) in mA.
Peak input current is 4.4 mA, peak input voltage is 1.5 V, with approximate impedance magnitude of 341 ohms at the 100 MHz signal frequency.

Fig. 5 illustrates a Keysight ADS large-signal s-parameter simulation of the configuration of Fig. 1 and schematic of Fig. 3, with T=1 ns and C = -5 pF. The dashed curve is real part of input impedance Z(s), and solid curve is imaginary part of input impedance Z(s). The predicted impedance is +j318 ohms for -5 pF at 100 MHz, and the observed impedance is -182 + j282 ohms at 100 MHz, or -5.6 pF in series with -182 ohms. In addition, the shape of the reactance follows the expected inverse frequency dependence of \( \text{Im}(Z(j \omega)) = \frac{1}{\omega(C)l} \) for a negative capacitor.

At low frequencies, the example implementation of Fig. 3 has a predictable and controllable series resistance, where \( Z(s) = I(s)V(s) = \left\{ s \frac{T}{(1 - z^{-1})H(z)} \right\}_{Z=exp(sT)} = \left\{ s \frac{T}{(1 - z^{-1}) (C(1 - z^{-1})/T)} \right\}_{Z=exp(sT)} = s T^2 ((sT)^2 C e^{s T}) \right\} = \frac{e^{j \omega T}}{j \omega C} \approx \frac{1}{j \omega C} + T/C. \) And so the parasitic resistance \( R_p \) at low frequency is approximately \( R_p \approx T/C, \) which in Fig. 3 and Fig. 5 would be \( R_p \approx -10^{-9}(-5 \times 10^{-12}) = -200 \) ohms, quite close to the low frequency value in Fig. 5. The designer is then free to reduce the magnitude of the low-frequency parasitic resistance by reducing \( T \) or increasing \( C. \) To illustrate this design freedom, the circuit of Fig. 3 is modified to reduce the series resistance by increasing the clock to 2 GHz, so \( T=0.5 \) ns, and increasing transconductance of SRC4 to 0.01 S, so that the capacitance remains at \( C = -5 \) pF, as before. Simulation results of the modified circuit are shown in Fig. 6, where the magnitude of the resistance at low frequency is reduced with \( Z = -69 + j315 \) ohms at 100 MHz, compared to the previous value of -182 + j282 ohms in Fig. 5. It should be understood that the designer may further compensate for desired Foster and non-Foster impedance characteristics as a function of frequency by proper design of \( H(z) \) using a variety of methods such as least-squares, Padé methods, Prony methods, bilinear transform, impulse invariance, and other such design methods for \( H(z). \)

Fig. 6 illustrates a Keysight ADS large-signal s-parameter simulation of the configuration of Fig. 1 and schematic of Fig. 3, modified with \( T=0.5 \) ns and \( C = -5 \) pF. The dashed curve is real part of input impedance \( Z(s), \) and the blue curve is imaginary part of input impedance \( Z(s). \) The predicted impedance is approximately \(+j318 \) ohms for \(-5 \) pF at 100 MHz, and the observed impedance is \(-69 + j315 \) ohms at 100 MHz, or \(-5.1 \) pF in series with \(-69 \) ohms. In addition, the shape of the reactance follows the expected inverse frequency dependence of \( \text{Im}(Z(j \omega)) = \frac{1}{\omega(C)l} \) for a negative capacitor.

Fig. 7 illustrates an Keysight ADS simulation schematic of the configuration of Fig. 1, with delay lines, switch, and hold capacitor \( C_1 \) used to simulate sampling at 1 GHz, \( T=1 \) ns, with \( |n| = |n-1| + T/v[n)L = |n-1| - 0.004 v[n], \) so design value is \( L = -T/1.004 = -250 \) nH. Figure 8 illustrates an Keysight ADS large-signal s-parameter simulation of the configuration of Fig. 1 and schematic of Fig. 7, for \( T=1 \) ns and \( L = -250 \) nH. The dashed curve is real part of input impedance \( Z(s), \) and the solid curve is imaginary part of input impedance \( Z(s). \) The predicted impedance is approximately \(-j157 \) ohms for \(-250 \) nH at 100 MHz, and the observed impedance is \(-14 - j137 \) ohms at 100 MHz, or \(-217 \) nH in series with \(-14 \) ohms. In addition, the shape of the reactance follows the expected frequency dependence of \( \text{Im}(Z(j \omega)) = -\omega |L| \) for a negative inductor. More details of Figures 7-8 are described below.
An example negative inductance implementation of the configuration of Fig. 1 is illustrated in the Keysight ADS schematic of Fig. 7. The Keysight ADS software offers large signal s-parameters for microwave impedance measurement, but does not appear to have convenient means for mixed-signal simulation; therefore, the ADCv of Fig. 1 is implemented as switch V1 and hold capacitor C1 in Fig. 7, the unit delay is simulated by 1 ns delay line TLD1, the discrete-time sum \( i[n] = i[n-1] + T v[n] \) is performed by voltage-controlled voltage source SRC3, voltage-controlled voltage source SRC6 with gain 0.004 establishes the value of \( T/L \), and finally the DACi is implemented with voltage-controlled current source SRC4 having transconductance 1 S. SRC7 and SRC10 are unity-gain voltage buffers, and the input of delay line TLD1 corresponds to \( i[n] \) and output of TLD1 corresponds to \( i[n-1] \). The switch V1 and hold capacitor C1 are used under control of clock oscillator SRC5 to simulate sampling at 1 GHz, and \( T=1 \) ns. From the foregoing theory for an inductance L, \( i[n] = i[n-1] + T v[n]/L \), and in the circuit of Fig. 3, \( i[n] = [i[n-1] - 0.004 v[n]] \), resulting a design value of \( L = -T/0.004 = -250 \) nH. The Keysight ADS large-signal s-parameter simulation of the configuration of Fig. 1 and schematic of Fig. 7 is shown in Fig. 8. The dashed curve is the real part of the input impedance \( Z(s) \), and the solid curve is the imaginary part of the input impedance \( Z(s) \). The predicted impedance is approximately \(-157 \) ohms for -250 nH at 100 MHz, and the observed impedance is \(-14 \) - j137 ohms at 100 MHz, or -217 nH in series with -14 ohms. In addition, the shape of the reactance follows the expected frequency dependence of \( \text{Im}(Z(j\omega)) = -\omega L \) for a negative inductor. The predicted parasitic resistance is zero for this implementation, since \( Z(s) = [sT][(1 - z^{-1})H(z)]e^{z^{-1}(sT)} = [sT][(1 - z^{-1}) T/(L - z^{-1}L)]e^{z^{-1}(sT)} = sL \), and so the simulation results show a small parasitic resistance of only -14 ohms at 100 MHz in Fig. 8.

Fig. 9 illustrates a Keysight ADS simulation schematic of the configuration of Fig. 2, with delay lines, switch, and hold capacitor C1 used to simulate sampling at 1 GHz, \( T=1 \) ns, with \( v[n] = L ((i[n] - i[n-1])/T = -200 \) \((i[n] - i[n-1]) \) so design value is \( L = -200 \) T = -200 nH. Fig. 10 illustrates a Keysight ADS large-signal s-parameter simulation of the configuration of Fig. 1 and schematic of Fig. 9, with \( T=1 \) ns and \( L = -200 \) nH. The dashed curve is real part of input impedance \( Z(s) \), and solid blue curve is imaginary part of input impedance \( Z(s) \). The predicted impedance is approximately \(-126 \) ohms for -200 nH at 100 MHz, and the observed impedance is \(-24 \) - j102 ohms at 100 MHz, or -162 nH in series with -24 ohms. In addition, the shape of the reactance follows the expected frequency dependence of \( \text{Im}(Z(j\omega)) = -\omega L \) for a negative inductor. More details of Figures 9-10 are discussed below.

An example negative inductance implementation of the configuration of Fig. 2 is illustrated in the Keysight ADS schematic of Fig. 9. The Keysight ADS software offers large signal s-parameters for microwave impedance measurement, but does not appear to have convenient means for mixed-signal simulation; therefore, the ADCi of Fig. 2 is implemented as switch V1 and hold capacitor C1 in Fig. 9 driven by voltage-controlled voltage source SRC10 with 1 ohm input impedance and unity voltage gain (converting current (I) into a voltage signal), the unit delay is simulated by 1 ns delay line TLD1, the discrete-time subtraction \( [i[n]-[i[n-1]] \) is performed by voltage-controlled voltage source SRC3, and finally the DACv is implemented with voltage-controlled voltage source SRC12 having a voltage gain of -200. SRC6 and SRC7 are unity-gain voltage buffers, and the input of delay line TLD1 corresponds to \( i[n] \) and output of TLD1 corresponds to \( i[n-1] \). The switch V1 and hold capacitor
C1 are used under control of clock oscillator SRC5 to simulate sampling at 1 GHz, and T=1 ns. From the foregoing theory of Fig. 2, the circuit of Fig. 9 implements an inductance where \( v[n] = L \left( (i[n] - i[n-1]) / T \right) = -200 (i[n] - i[n-1]) \), corresponding to a design value \( L = -200 \) T = -200 nH. Fig. 10 shows a Keysight ADS large-signal s-parameter simulation of the configuration of Fig. 2 and schematic of Fig. 9, with T=1 ns and L = -200 nH. The dashed curve in Fig. 10 is the real part of the input impedance Z(s), and the solid curve is the imaginary part of the input impedance Z(s). The predicted impedance is approximately \(-j126\) ohms for -200 nH at 100 MHz, and the observed impedance is \(-24 \text{--} j102\) ohms at 100 MHz, or \(-162\) nH in series with \(-24\) ohms. In addition, the shape of the reactance (blue curve) in Fig. 10 follows the expected frequency dependence of \( \text{Im}[Z(j\omega)] = -\omega|L| \) for a negative inductor. The predicted parasitic resistance follows from the relation \( Z(s) = \left\{ \text{H}(z)(1 - z^{-1})/(sT) \right\}_{z=\exp(i\omega T)} = (L (1 - z^{-1})/(sT))_{z=\exp(i\omega T)} = -71 - j98 \), in agreement with the simulation results of \(-24 \text{--} j102\) ohms at 100 MHz.

[0052] Fig. 11 shows a Keysight ADS simulation schematic of the configuration of Fig. 2, with delay lines, switch, and hold capacitor C1 used to simulate sampling at 1 GHz, T=1 ns, with \( v[n] = v[n-1] + T \left( i[n] / C \right) = v[n-1] - 200 \) [n], so the design value is \( C = T / 200 = -5 \) pF. More details of Figure 11 is discussed below.

[0053] An example negative capacitance implementation of the configuration of Fig. 2 is illustrated in the Keysight ADS schematic of Fig. 11. The Keysight ADS software offers large signal s-parameters for microwave impedance measurement, does not haveHad an effective means for mixed-signal simulation; therefore, the ADC of Fig. 2 is implemented as switch V1 and hold capacitor C1 in Fig. 11 driven by voltage-controlled voltage source SRC10 with 1 ohm input impedance and unity voltage gain (converting current i(t) into a voltage signal), the unit delay is simulated by 1 ns delay line TLD1, the discrete-time addition \( v[n-1] + T \left( i[n] / C \right) \) is performed by voltage-controlled voltage source SRC3, and finally the DACv is implemented with voltage-controlled voltage source SRC12 having a voltage gain of 1. SRC6 has gain 200 to establish T/C, and SRC7 is unity-gain voltage buffer, and the input of delay line TLD1 corresponds to \( v[n] \) and output of TLD1 corresponds to \( v[n-1] \). The switch V1 and hold capacitor C1 are used under control of clock oscillator SRC5 to simulate sampling at 1 GHz, and T=1 ns, with the output of the switch representing \( i[n] \). From the foregoing theory of Fig. 2, the circuit of Fig. 11 implements capacitance by \( v[n] = v[n-1] + T \left( i[n] / C \right) = v[n-1] - 200 \) [n], corresponding to a design value \( C = -T / 200 = -5 \) pF. Fig. 12 shows a Keysight ADS large-signal s-parameter simulation of the configuration of Fig. 2 and schematic of Fig. 11, with T=1 ns and C = -5 pF. The dashed red curve in Fig. 12 is the real part of the input impedance Z(s), and the solid blue curve is the imaginary part of the input impedance Z(s). The predicted impedance is \(+j318\) ohms for -5 pF at 100 MHz, and the observed impedance is \(9 + j292\) ohms at 100 MHz, or -5.5 pF in series with 9 ohms. In addition, the shape of the reactance follows the expected inverse frequency dependence of \( \text{Im}[Z(j\omega)] = +1/(\omega C) \) for a negative capacitor. Predicted parasitic resistance is zero for this implementation, since \( Z(s) \approx \left\{ \text{H}(z)(1 - z^{-1})/(sT) \right\}_{z=\exp(i\omega T)} = \left\{ \left( T / (C - z^{-1} C) \right) (1 - z^{-1})/(sT) \right\}_{z=\exp(i\omega T)} = 1 / (s C) \), the simulation results show only 9 ohms parasitic resistance at 100 MHz from Fig. 12. Fig. 13 illustrates an embodiment with adaptive control, where continous-time input voltage \( v(t) \) is digitized by analog-to-digital converter ADCv into discrete-time signal \( v[n] \), then processed by a discrete-time filter with \( z \)-transform \( H(z) \) to form discrete-time signal \( y[n] \), an adaptive controller with input \( v[n] \) and with output discrete-time signal e[n] and
with output control bus B that controls \( H(z) \), and an adder that forms discrete-time current \( i[n] = y[n]+e[n] \) which is finally converted into continuous-time input current \( i(t) \) by digital-to-analog converter DACi. As illustrated, ADCv would have high input impedance, and DACi would have high output impedance.

[0054] It should be understood that the signal processing and discrete time approach of the present application offers significant advantages such as low cost, repeatability, scalability, and incorporation of adaptive control methods and adaptive stabilization methods. It should be understood that signal processing and discrete time approaches can be implemented in analog hardware, in delay lines, in analog signal samplers, in digital circuits, in software, or in combinations of these means. An embodiment with adaptive control is shown in Fig. 13, where continuous-time input voltage \( v(t) \) with Laplace transform \( V(s) \) is digitized by ADCv into discrete-time signal \( v[n] \), then processed by a discrete-time filter with impulse response \( h[n] \) and z-transform \( H(z) \) to form discrete-time signal \( y[n] = v[n]*h[n] \), (with \( * \) denoting convolution). An adaptive controller with input \( y'[n] \) has an output discrete-time signal \( e[n] \) and has an output control bus B that controls \( H(z) \) and \( h[n] \). An adder generates discrete-time current \( i[n] = y'[n]+e[n] \), and \( i[n] \) is finally converted by DACi into continuous-time input current \( i(t) \) with Laplace transform \( I(s) \). As illustrated in Fig. 9, ADCv would have high input impedance, and DACi high output impedance. It should be understood that the embodiment of Fig. 13 is an adaptive controlled version of the embodiment of Fig. 1, and similar adaptive controlled embodiments can be created for the embodiment of Fig. 2.

[0055] It should be understood that the adaptive controller of Fig. 13 can be used to accomplish a wide variety of desirable system behaviors such as system adaptation to changing input signals, adaptation to changing external impedances, adaptation to changing temperature, and adaptive stabilization methods. Of particular interest in many non-Foster circuit applications is the use of the adaptive controller of Fig. 13 for adaptive stabilization methods to assure stability in the presence of an external load impedance \( Z_a(s) \). Under these conditions, the total impedance \( Z_t(s) \) at the port terminal is the parallel combination \( Z_t(s) = Z_a(s) Z(s) / [Z_a(s) + Z(s)] \), where \( Z(s) = V(s)/I(s) \). The embodiment of Fig. 13 can be used to stabilize \( Z_t(s) \) in a variety of ways. In one example implementation, an initialization sequence can be used to first probe \( Z_a(s) \) where the adaptive controller in Fig. 13 initially sets \( H(z) = 0 \) and \( h[n] = 0 \) such that \( y[n] = 0 \), and then applies an impulse \( e[n] \) such that \( i[n] = y[n] + \delta[n] = \delta[n] \) initially. The adaptive controller then measures the voltage response \( v[n] \) to determine \( Z_a(s) \), since \( V^*(s) = \sum V(nT)e^{-ns} \approx V(s) \approx Z_a(s) \) below the Nyquist frequency 0.5/T Hz for an impulse current at \( i[n] \). In many non-Foster applications, a non-Foster impedance \( Z(s) \) is used to obtain some desired stable total impedance \( Z_t(s) \), for example cancelling some external capacitance. In such applications where the desired stable \( Z_t(s) \) is known and where \( Z_a(s) \) is determined from the foregoing initialization, the necessary design impedance is \( Z(s) = V(s)/I(s) = Z_a(s) Z_t(s) / [Z_a(s) - Z_t(s)] \). When \( e[n] = 0 \) after initialization for the configuration of Fig. 13, the desired \( H(z) \) is then established by the adaptive controller over control bus B. For example, noting that \( I(z) = H(z) V(z) \) in Fig. 13, \( H(s) \) could be determined using the bilinear transform method, \( H(z) = I(z) / V(z) = Z^{-1}(s) = \{ [Z_a(s) - Z_t(s)] / [Z_a(s) Z_t(s)] \} (s^2 + T^2 z^{-1} + T z^{-1}) \). It should be understood that the design can also be modified to compensate for a zero order hold in the DACi. It should be understood that a variety of alternative methods such as least-squares, Pade methods, Prony methods, impulse invariance, and other such design methods can be used to design \( H(z) \). It is also noted that use of the autocorrelation method form of Prony filter
design in implementations of the foregoing procedures results in Toeplitz form normal equations, assuring stable discrete-time designs with poles inside the unit circle. It should be understood that many other techniques may be used to establish $H(z)$ and stability of the overall system, even in non-stationary environments, including pseudo-random training sequences, least mean squares, recursive least squares, Kalman filtering, and many other adaptive filter design methods.

[0056] As an example of the foregoing method, consider an external impedance of a positive resistance $R$ in parallel with a positive capacitance $C$, such that $Z_d(s) = R/(1 + sRC)$ and where a desired total impedance $Z_r(s) = R/(1 + sR(C/10))$ is the design goal. This is the equivalent of reducing the external capacitance $C$ by a factor of 0.9. The external impedance would first be determined, as described above, by setting $H(z)=0$ and applying an impulse $i[n] = \delta[n]$, and determining $Z_d(s)$ from the measured $v[n]$. The desired design impedance is then $Z(s) = V(s)/I(s) = Z_d(s) Z_r(s)/(Z_d(s) - Z_r(s)) = -1/(0.9 sC)$. In essence, the design results in a negative capacitor of -0.9 C to be placed in parallel with the external load of $R$ in parallel with capacitance $C$. Since the result for this example is a negative capacitor, the methods of designing $H(z)$ for negative capacitance in the previous paragraphs, and in following paragraphs, can also be used.

[0057] A two-port embodiment of the present application is shown in Fig. 14. The one-port embodiments of Fig. 1, Fig. 2, and Fig. 13 are further extended to multiport designs, such as the two-port example of Fig. 14. In Fig. 14, a two-port embodiment has continuous-time input voltages $v_1(t)$ and $v_2(t)$ that are digitized by two analog-to-digital converters denoted ADC into discrete-time signals $v_1[n]$ and $v_2[n]$, then processed by a multiport discrete-time filter with z-transform admittance matrix $Y(z)$ to form discrete-time currents $i_1[n]$ and $i_2[n]$, which are finally converted into continuous-time input currents $i_1(t)$ and $i_2(t)$ by two digital-to-analog converters denoted DACi. As illustrated, the two ADCs would have high input impedances, and the two DACs would have high output impedances.

[0058] In the two-port embodiment illustrated in Fig. 14, analog continuous-time input voltages $v_1(t)$ and $v_2(t)$ with Laplace transforms $V_1(s)$ and $V_2(s)$ are converted to digital discrete-time signals $v_1[n]$ and $v_2[n]$ with z-transforms $V_1(z)$ and $V_2(z)$ by a pair of analog-to-digital voltage converters (ADCv) with clock period $T$, processed digitally with a multi-port discrete-time filter with z-transform admittance matrix $Y(z)$ to form discrete-time signals $i_1[n]$ and $i_2[n]$ having z-transforms $I_1(z)$ and $I_2(z)$, and finally $i_1[n]$ and $i_2[n]$ are converted into analog continuous-time input currents $i_1(t)$ and $i_2(t)$ having Laplace transform $I_1(s)$ and $I_2(s)$ by using two digital-to-analog current converters (DACi) with clock period $T$. The z-transform admittance matrix $Y(z)$ is defined as:

$$
\begin{bmatrix}
I_1(z) \\
I_2(z)
\end{bmatrix} =
\begin{bmatrix}
Y_{11}(z) & Y_{12}(z) \\
Y_{21}(z) & Y_{22}(z)
\end{bmatrix}
\begin{bmatrix}
V_1(z) \\
V_2(z)
\end{bmatrix} = Y(z)
\begin{bmatrix}
V_1(z) \\
V_2(z)
\end{bmatrix}
$$

(1)

[0059] where the z-transform relations are $I_1(z) = V_1(z)Y_{11}(z) + V_2(z)Y_{12}(z)$ and $I_2(z) = V_1(z)Y_{21}(z) + V_2(z)Y_{22}(z)$, with corresponding convolution relations $i_1[n] = v_1[n] * h_1[n] + v_2[n] * h_2[n]$ and $i_2[n] = v_1[n] * h_3[n] + v_2[n] * h_2[n]$ (with * denoting convolution). For this embodiment,

[0060] $I_1(s) = V_1^*(s) \{ Y_{11}(z) (1 - z^*)/s \} \mid_{z = \exp(sT)} + V_2^*(s) \{ Y_{12}(z) (1 - z^*)/s \} \mid_{z = \exp(sT)}$

[0061] And

$$\quad$$

[0062] And
\[ I_t(s) = V_1(t) \{ Y_{21}(z) (1 - z^{-1}) / s \}_{z=exp(st)} + V_2(t) \{ Y_{22}(z) (1 - z^{-1}) / s \}_{z=exp(st)} \]

And so,

\[
\begin{bmatrix}
I_1(s) \\
I_2(s)
\end{bmatrix} =
\begin{bmatrix}
\frac{Y_{11}(z)(1 - z^{-1})}{s} \big|_{z=exp(st)} & \frac{Y_{12}(z)(1 - z^{-1})}{s} \big|_{z=exp(st)} \\
\frac{Y_{21}(z)(1 - z^{-1})}{s} \big|_{z=exp(st)} & \frac{Y_{22}(z)(1 - z^{-1})}{s} \big|_{z=exp(st)}
\end{bmatrix}
\begin{bmatrix}
V_1(s) \\
V_2(s)
\end{bmatrix}
\]

(2)

where \( V^*(s) = \sum v(nT)e^{-nsT} \) for integer \( n \), and assuming a zero-order hold (ZOH) incorporated into the DACi.

To illustrate the embodiment of Fig. 14, consider the example of implementing a two-port circuit that simply consists of capacitor connected between the two ports, with capacitance \( C \). In this example the Laplace admittance matrix \( Y(s) \) and equations for the analog circuit are:

\[
\begin{bmatrix}
I_1(s) \\
I_2(s)
\end{bmatrix} =
\begin{bmatrix}
sC & -sC \\
-sC & sC
\end{bmatrix}
\begin{bmatrix}
V_1(s) \\
V_2(s)
\end{bmatrix} = Y(s)
\begin{bmatrix}
V_1(s) \\
V_2(s)
\end{bmatrix}
\]

(3)

For this example of a capacitor connected between the two ports, the currents are \( i_1(t) = -i_2(t) = C \frac{d}{dt} (v_1(t) - v_2(t)) \), and a positive or negative capacitor may be approximated in the embodiment of Fig. 14 by using the discrete-time backward-difference approximation of the derivative

\[ i[n] = -i_2[n] = C (v_1[n] - v_2[n] - v_1[n-1] + v_2[n-1]) / T, \]

(4)

or equivalently setting

\[ I_1(z) = -I_2(z) = C V_1(z) (1 - z^{-1}) / T - C V_2(z) (1 - z^{-1}) / T. \]

Thus, the two-port admittance matrix \( Y(z) \) and relations become:

\[
\begin{bmatrix}
I_1(z) \\
I_2(z)
\end{bmatrix} =
\begin{bmatrix}
\frac{C}{T}(1 - z^{-1}) & -\frac{C}{T}(1 - z^{-1}) \\
-\frac{C}{T}(1 - z^{-1}) & \frac{C}{T}(1 - z^{-1})
\end{bmatrix}
\begin{bmatrix}
V_1(z) \\
V_2(z)
\end{bmatrix} = Y(z)
\begin{bmatrix}
V_1(z) \\
V_2(z)
\end{bmatrix}
\]

(4)

As illustrated in Fig. 14 and the foregoing example, preferentially the two ADCv would have high input impedances and the two DACi would have high output impedance, for simplicity in exposition, such that the current into the two ADCv would be approximately zero and the port currents approximately equal to the DACi output currents. Alternatively, the positive or negative capacitor may be approximated by using the bilinear transform approximation on the matrix \( Y(s) \) in (3), replacing \( s \) by \( 2(z - 1) / (z + 1) \) \( T \) yielding:

\[
\begin{bmatrix}
I_1(z) \\
I_2(z)
\end{bmatrix} =
\begin{bmatrix}
\frac{2C(z - 1)}{T(z + 1)} & -\frac{2C(z - 1)}{T(z + 1)} \\
\frac{2C(z - 1)}{T(z + 1)} & \frac{2C(z - 1)}{T(z + 1)}
\end{bmatrix}
\begin{bmatrix}
V_1(z) \\
V_2(z)
\end{bmatrix}
\]

(5)

It should be understood that any general Foster or non-Foster two-port with admittance matrix \( Y(s) \) may be approximated by appropriate selection of discrete-time signal processing system characterized by two-port \( z \)-transform admittance matrix \( Y(z) \), where such discrete-time signal processing may be accomplished in hardware,
software, or combination of hardware and software. It should be understood that the foregoing one and two-port embodiments of Foster or non-Foster circuits can be extended to any number of ports. It should be understood that the designer may further compensate for desired Foster and non-Foster two-port characteristics as a function of frequency by proper design of admittance matrix \( Y(z) \) using a variety of methods such as least-squares, Padé methods, Prony methods, bilinear transform, impulse invariance, and other such design methods for \( H(z) \). It should be understood that admittance matrices may be converted to and from other types of matrices such as impedance matrices, ABCD matrices, and other forms as may be useful for a particular application or design. It should be understood that the embodiment of Fig. 2 when adapted to the two-port embodiment of Fig. 14 would result more naturally in a z-transform impedance matrix \( Z(z) \), as illustrated in Fig. 15. The z-transform impedance matrix \( Z(z) \) is defined as:

\[
\begin{bmatrix}
  V_1(z) \\
  V_2(z)
\end{bmatrix}
= 
\begin{bmatrix}
  Z_{11}(z) & Z_{12}(z) \\
  Z_{21}(z) & Z_{22}(z)
\end{bmatrix}
\begin{bmatrix}
  I_1(z) \\
  I_2(z)
\end{bmatrix}
= Z(z)
\begin{bmatrix}
  I_1(z) \\
  I_2(z)
\end{bmatrix}
\]  

(6)

[0079] It is noted that Fig. 15 illustrates a second two-port embodiment where continuous-time input currents \( i_1(t) \) and \( i_2(t) \) are digitized by two ADCs into discrete-time signals \( i_1[n] \) and \( i_2[n] \), then processed by a multi-port discrete-time filter with z-transform impedance matrix \( Z(z) \) to form discrete-time signals \( v_1[n] \) and \( v_2[n] \), which are finally converted into continuous-time output voltages \( v_1(t) \) and \( v_2(t) \) by two DACs. As illustrated, ADC would have low input impedance, and DACs low differential output impedance, and \( i[n] = i(nT) \) for integer \( n \) and clock period \( T \).

[0080] Fig. 16 illustrates an Keysight ADS simulation schematic an implementation of the two-port configuration of Fig. 14, designed to implement a capacitance between the two ports, with sampling at 1 GHz, \( T=1 \) ns, with \( i_1[n] = i_2[n] = C(v_1[n] - v_2[n] - v_1[n-1] + v_2[n-1]) \) \( T = -0.005 \) \( v_1[n] - v_2[n] - v_1[n-1] + v_2[n-1] \), so design value is \( C = 0.005 \) \( T = -5 \) pF. The implementation is based on the one-port design of Fig. 3, replicated to support two ports and share a common clock. More information on Figure 16 is discussed below.

[0081] An example negative capacitance implementation of the configuration of Fig. 14 is illustrated in the Keysight ADS schematic of Fig. 16. The Keysight ADS software offers large signal s-parameters for microwave impedance measurement, but does not appear to have convenient means for mixed-signal simulation; therefore, the two DACs of Fig. 14 are implemented as switches V1 and V2 and hold capacitors C1 and C2 in Fig. 16, the unit delay is simulated by 1 ns delay lines TLD1 and TLD4, the discrete-time subtraction \( v_1[n] - v_2[n] - v_1[n-1] + v_2[n-1] \) is performed by voltage-controlled voltage sources SRC3, SCR16, and SRC18, and finally the two DACs are implemented with voltage-controlled current sources SRC4 and SRC17 having transconductance 0.005 S. SRC19 drives SRC17 out of phase to accomplish the relationship \( i_1[n] = -i_2[n] \) in the design equation \( i_1[n] = -i_2[n] = C (v_1[n] - v_2[n] - v_1[n-1] + v_2[n-1]) / T \). SRC6, SRC7, SRC10, SRC13, SRC14, and SRC15 are unity-gain voltage buffers, and the inputs of delay lines TLD1 and TLD4 correspond to \( v_1[n] \) and \( v_2[n] \) and outputs correspond to \( v_1[n-1] \) and \( v_2[n-1] \). The switches V1 and V2 and hold capacitors C1 and C2 are used under control of clock oscillator SRC5 to simulate sampling at 1 GHz, and \( T=1 \) ns. The two ports of Fig. 14 correspond to the two terminals of the floating differential input denoted P_.1Tone PORT1 in the Fig. 16 schematic, and corresponds to
a differential excitation across the two ports. From the foregoing theory for a two-port network equivalent to a capacitance $C$ connected between the ports, \[ i_1[n] = -i_2[n] = C(v_1[n] - v_2[n] - v_1[n-1] + v_2[n-1])/T, \]
and in the circuit of Fig. 16, \[ i_1[n] = -i_2[n] = -0.005 (v_1[n] - v_2[n] - v_1[n-1] + v_2[n-1]), \]
resulting a design value of $C = -0.005 \text{ pF}$.

[0082] Fig. 17 shows a Keysight ADS large-signal s-parameter simulation of the configuration of Fig. 14 and schematic of Fig. 16, with $T=1$ ns and $C = -5 \text{ pF}$. The dashed curve is the real part of the differential input impedance between the two ports, and the solid curve is the imaginary part of the input impedance. The predicted impedance is approximately $+j318$ ohms for $-5 \text{ pF}$ at 100 MHz, and the observed impedance of $-181 + j283$ ohms at 100 MHz corresponds to 5.6 pF in series with $-181$ ohms. The predicted value of parasitic resistance can be calculated from the relation $Z(s) = \{sT/(1 - z^{-1}) H(z)\}\{z^{-\exp(\alpha T)} = \{sT/(1 - z^{-1}) C(1 - z^{-1})/T]\\{z^{-\exp(\alpha T)} = -193 + j266$, and is in good agreement with the simulation results of $-181 + j283$ ohms at 100 MHz. In addition, the shape of the reactance (solid blue curve) in Fig. 17 follows the expected inverse frequency dependence of $\text{Im}(Z(j\omega)) = \pm 1/(\alpha|C|)$ for a negative capacitor.

[0083] In the foregoing two-port and multi-port embodiments, it is also noted that use of the autocorrelation method form of Prony filter design in implementations of the foregoing procedures results in Toeplitz form normal equations, assuring stable discrete-time filter designs with poles inside the unit circle. It should be understood that many other techniques may be used to establish z-transform admittance matrices $Y(z)$ and z-transform impedance matrices $Z(z)$ and establish stability of the overall system, even in non-stationary environments, including pseudo-random training sequences, least mean squares, recursive least squares, Kalman filtering, and many other adaptive filter design methods.

[0084] The invention is also of general use in electronic circuits, and in particular digital discrete-time implementation of Foster and non-Foster circuits. Non-Foster circuits are of particular interest in electromagnetics, metamaterials, and antenna applications. Such non-Foster circuits are useful to increase bandwidth of systems and to perform functions not possible in naturally occurring circuits and devices such as conventional capacitors, inductors, dielectrics, antennas, and ferrites.

[0085] Figures 18-19 provide an overview of digital non-Foster circuits and elements thereof according some embodiments of the present application.

[0086] Fig. 18 illustrates a single-port embodiment of the arrangement of Fig. 1, where continuous-time input voltage $v(t)$ at one port is digitized by the Voltage-Input Analog-to-Digital Converter into discrete-time signal $v[n]$, then processed by a Digital Signal Processor (DSP) to form discrete-time signal $i[n]$, which is finally converted into continuous-time input current $i(t)$ by the Current-Output Digital-to-Analog Converter. As illustrated, the Voltage-Input Analog-to-Digital Converter (ADCv) would have high input impedance, and the Current-Output Digital-to-Analog Converter (DACi) would have high output impedance, and $v[n]=v(nT)$ and $i(nT)=i[n]$ for integer $n$ and clock period $T$. The ADCv receives the continuous-time input signal, voltage signal $v(t)$, from the circuit port. A discrete-time input signal $v[n]$ is then outputted by the ADCv.

[0087] The DSP then receives the discrete-time input signal $v[n]$ and outputs a discrete-time output signal $i[n]$. In a typical embodiment of Fig. 18, the Digital Signal Processor would implement a discrete-time filter having impulse response $h[n]$ with z-transform $H(z)$, where $i[n]=v[n]*h[n]$ (with * denoting convolution), and with
corresponding difference equation representations such as \( i[n] = C (v[n] - v[n-1])/T \) for a positive or negative capacitance \( C \). It should be understood that the present invention should not be limited by any particular elements in the DSP as long as the discrete-time input signal \( v[n] \) is received and converted into a discrete-time output signal \( i[n] \) (e.g., \( v[n] \rightarrow i[n] \) as shown in Fig. 18, or alternatively \( i[n] \rightarrow v[n] \) as shown in Figure 19).

[0088] The DACi then receives the discrete-time output signal \( i[n] \), converts such digital signal \( i[n] \) to an analog continuous-time output signal current, current signal \( i(t) \), and outputs the desired current \( i(t) \) to the same port as continuous-time input signal \( v(t) \). In one embodiment, the node at the input of the ADCv is the same node as the output of the DACi. In another embodiment with two or more ports, every one of the ports is connected to the input of an ADCv and to the output of a DACi as illustrated for the single port in the embodiment of Figure 18. As illustrated in Fig. 18, preferentially the ADCv would have high input impedance and the DACi would have high output impedance, for simplicity in exposition, such that the current into the ADCv would be approximately zero and the port current would approximately equal the DACi output current.

[0089] Fig. 19 shows an alternate embodiment to Figure 18 and illustrates a single-port embodiment of the arrangement of Fig. 2. Indeed, continuous-time input signal, input current \( i(t) \), is received from the single port and digitized by the Current-Input Analog-to-Digital Converter (ADCi) into discrete-time input signal \( i[n] \). Then, the outputted discrete-time input signal \( i[n] \) is received by and processed by a Digital Signal Processor to output a discrete-time output signal \( v[n] \). The outputted discrete-time output signal \( v[n] \) is received by and converted into continuous-time output signal voltage, voltage \( v(t) \), by the Voltage-Output Digital-to-Analog Converter (DACv), which provides the desired voltage \( v(t) \) back to the, where the voltage drop across the ADCi is preferentially negligible for a preferentially low impedance ADCi and low impedance DACv.

[0090] As illustrated in Fig. 19, the Current-Input Analog-to-Digital Converter would have low input impedance, and the Voltage-Output Digital-to-Analog Converter would have low output impedance, the voltage drop across the ADCi is preferentially negligible, and \( v(nT)=v[n] \) and \( i(nT)=i[n] \) for integer \( n \) and clock period \( T \).

[0091] In a typical embodiment of Fig. 19, the Digital Signal Processor would implement a discrete-time filter having impulse response \( h[n] \) with z-transform \( H(z) \), where \( v[n]=v[n]*h[n] \) (with \( * \) denoting convolution), and with corresponding difference equation representations such as \( v[n] = L ([i[n] - i[n-1])/T \) for a positive or negative inductance \( L \).

[0092] Fig. 20 illustrates a broad or generic flow chart illustrating an embodiment of the present application. In step 202, an observed continuous-time input voltage \( v(t) \) from one or more ports of a circuit are digitized at an input signal port by means of a voltage-input analog-to-digital converter to form a sampled discrete-time input signal \( v[n] \) where \( v[n] = v(nT) \) for sampling period \( T \), and where the analog-to-digital converter may have a high impedance.

[0093] In step 204, the sampled discrete-time input signal, or vector, or multiplicity of signals is processed (by means such as digital signal processors, digital logic, analog computers, or digital computers) to calculate a desired discrete-time output signal.

[0094] It should be understood that the processing is to include functionality such as convolution, admittance matrices, impedance matrices, nonlinearity, adaptive behavior, and time-variance as desired;
In step 206, the discrete-time output signal of the DSP, for example, is then converted by a digital-to-analog converter which outputs a desired continuous-time output signal current to the one or more ports, such as desired port currents for given port voltages, or desired port voltages for given port currents.

In step 208, the one or more ports receives the desired continuous-time outputted signal of the digital-to-analog converter while also providing the continuous-time input to the analog-to-digital converter.

Fig. 21 is a flow chart corresponding to Fig. 1, according to one embodiment. In step 302, an observed continuous-time input signal voltage $v(t)$ is digitized at a port by means of a voltage-input analog-to-digital converter to form a sampled discrete-time input signal $v[n]$, where $v[n] = v(nT)$ for sampling period $T$, and where said analog-to-digital converter preferably has high input impedance.

In step 304, the sampled discrete-time input signal $v[n]$, is processed by means such as digital signal processors, digital logic, analog computers, or digital computers to calculate a desired discrete-time output signal $i[n]$ at said port.

In step 306, the processing to be a discrete-time convolution where desired discrete-time output signal $i[n] = v[n] * h[n]$ (with $*$ denoting convolution), having impulse response $h[n]$ with z-transform $H(z)$ and corresponding difference equation representations, such as $i[n] = C \{ v[n] - v[n-1] \}/T$ for a positive or negative capacitance C.

In step 308, the calculated desired discrete-time output signal $i[n]$ is to be converted to continuous-time output signal current $i(t)$ at said port by means of a current-output digital-to-analog converter with sampling period $T$, where said digital-to-analog converter preferably has high output impedance.

Fig. 22 illustrates a flow chart corresponding to Fig. 2, according to one embodiment. In step 402, an observed continuous-time input signal current $i(t)$ is digitized at a port by means of a current-input analog-to-digital converter to form a sampled discrete-time input signal $i[n]$, where $i[n] = i(nT)$ for sampling period $T$, and where said analog-to-digital converter preferably has low input impedance.

In step 404, the sampled discrete-time input signal $i[n]$, is processed by means such as digital signal processors, digital logic, analog computers, or digital computers to calculate a desired discrete-time output signal $v[n]$ at said port.

In step 406, the processing to be a discrete-time convolution where desired discrete-time output signal $v[n] = i[n] * h[n]$ (with $*$ denoting convolution), having impulse response $h[n]$ with z-transform $H(z)$ and corresponding difference equation representations, such as $v[n] = L \{ i[n] - i[n-1] \}/T$ for a positive or negative inductance L.

In step 408, the calculated desired discrete-time output signal $v[n]$ to be converted to the continuous-time output signal voltage $v(t)$ at said port by means of a voltage-output digital-to-analog converter with sampling period $T$, where said digital-to-analog converter preferably has low output impedance.

Fig. 23 illustrates a flow chart corresponding to Fig.14, according to another embodiment. In step 502, an observed continuous-time input signal vector voltage $v(t)$ is digitized at two or more ports by means of voltage-input analog-to-digital converters at every port to form a sampled discrete-time input signal vector $v[n]$. 
where $v[n] = v(nT)$ for sampling period $T$, and where said analog-to-digital converters preferentially have high input impedances.

[00106] In step 504, the sampled discrete-time input signal vector $v[n]$, is processed by means such as digital signal processors, digital logic, analog computers, or digital computers to calculate a desired discrete-time output signal vector $i[n]$ at said ports.

[00107] In step 506, the processing may be a discrete-time convolution where the z-transform of the desired discrete-time output vector is determined from $I(z) = V(z)Y(z)$ and where the desired response is determined by z-transform admittance matrix $Y(z)$, with $I(z)$ being the z-transform of discrete-time output vector $i[n]$, and with $V(z)$ being the z-transform of discrete-time input vector $v[n]$.

[00108] In step 508, the calculated desired discrete-time output signal vector $i[n]$ may be converted to the continuous-time output signal vector current $i(t)$ at said ports by means of current-output digital-to-analog converters at every port with sampling period $T$, where said digital-to-analog converters preferentially have high output impedances.

[00109] The following are some embodiments of the present application:

[00110] A1. A method to implement circuits and circuit elements having one or more ports, comprising: digitizing, using an analog-to-digital converter, a signal at one or more ports of a component; processing the signal to calculate a desired current or voltage at the one or more ports; processing to include functionality comprising at least one of convolution, difference equations, admittance matrices, impedance matrices, nonlinearity, adaptive, and time-variance; and converting, using a digital-to-analog converter, the calculated desired current or voltage to output signal at one or more ports.

[00111] The method of claim A1, for non-Foster circuits and non-Foster elements.

[00112] The method of claim A2 where: said digitizing consists of digitizing the voltage at the port of a component having only one port; said processing consists of calculating the desired current at said port; said processing to include functionality comprising convolution or difference equations; and converting, using a digital-to-analog converter, the calculated desired current to output signal at said port.

[00113] The method of claim A3 where: said functionality comprises a difference equation $i[n] = C (v[n] - v[n-1]) / T$ for a preferentially negative capacitance $C$, relating desired port current $i[n]$ to digitized port voltage $v[n]$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter.

[00114] The method of claim A3 where: said functionality comprises a difference equation $i[n] = i[n-1] + C v[n] / L$ for a preferentially negative inductance $L$, relating desired port current $i[n]$ to digitized port voltage $v[n]$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter.

[00115] The method of claim A3 where: said functionality comprises a convolution relating desired port current $i[n]$ to digitized port voltage $v[n]$, where $i[n] = v[n] * h[n]$, with $*$ denoting convolution, where impulse response $h[n]$ has z-transform $H(z)$, and where $H(z) = 2C (z - 1)/(z + 1)T$ for a preferentially negative capacitance $C$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter.

[00116] The method of claim A3 where: said functionality comprises a convolution relating desired port current $i[n]$ to digitized port voltage $v[n]$, where $i[n] = v[n] * h[n]$, with $*$ denoting convolution, where impulse response $h[n]$
has z-transform $H(z)$, and where $H(z) = T(z+1)/\{2L(z-1)\}$ for a preferentially negative inductance $L$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter.

[00117] The method of claim A3 where: said functionality includes an adaptive method for determining the initial external impedance $Z_e(s)$ seen by the port by first generating a current impulse using said digital-to-analog converter, measuring the impulse response voltage using said analog-to-digital converter, taking $Ze(s) = i(nT)e^{-nsT}$, then computing desired processing functionality $H(z) = \{(Ze(s) - ZT(s))/(Ze(s)ZT(s))\}s(2T)(z-1)/(z+1)$, where $ZT(s)$ is the desired the total impedance at the port.

[00118] The method of claim A8 where: said functionality includes an adaptive method for determining the external impedance $Z_e(s)$ seen by the port by using a pseudorandom current instead of said current impulse.

[00119] The method of claim A2 where: said digitizing consists of digitizing the current at the port of a component having only one port; said processing consists of calculating the desired voltage at said port; said processing to include functionality comprising convolution or difference equations; and converting, using a digital-to-analog converter, the calculated desired voltage to output signal at said port.

[00120] The method of claim A10 where: said functionality comprises a difference equation $v[n] = L(i[n] - i[n-1])/T$ for a preferentially negative inductance $L$, relating desired port voltage $v[n]$ to digitized port current $i[n]$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter.

[00121] The method of claim A10 where: said functionality comprises a difference equation $v[n] = v[n-1] + T i[n]/C$ for a preferentially negative capacitance $C$, relating desired port voltage $v[n]$ to digitized port current $i[n]$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter.

[00122] The method of claim A10 where: said functionality comprises a convolution relating desired port voltage $v[n]$ to digitized port current $i[n]$, where $i[n]=v[n]+h[n]$, with * denoting convolution, where impulse response $h[n]$ has z-transform $H(z)$, and where $H(z) = 2L(z-1)/\{2L(z+1)\}$ for a preferentially negative inductance $L$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter.

[00123] The method of claim A10 where: said functionality comprises a convolution relating desired port voltage $v[n]$ to digitized port current $i[n]$, where $i[n]=v[n]+h[n]$, with * denoting convolution, where impulse response $h[n]$ has z-transform $H(z)$, and where $H(z) = T(z+1)/\{2C(z-1)\}$ for a preferentially negative capacitance $C$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter.

[00124] The method of claim A10 where: said functionality includes an adaptive method for determining the initial external impedance $Z_e(s)$ seen by the port by first generating a voltage impulse using said digital-to-analog converter, measuring the impulse response current using said analog-to-digital converter, then computing desired processing functionality $H(z)$.

[00125] The method of claim A15 where: said functionality includes an adaptive method for determining the external impedance $Z_e(s)$ seen by the port by using a pseudorandom current instead of said current impulse.

[00126] The method of claim A2 where: said digitizing consists of digitizing the voltages at every port of a component having two or more ports; said processing consists of calculating the desired current at every one of said ports; said processing to include functionality comprising an z-transform admittance matrix $Y(z)$; and
converting, using a digital-to-analog converter, the calculated desired currents to output signal at every one of said ports.

[00127] The method of claim A2 where: said digitizing consists of digitizing the currents at every port of a component having two or more ports; said processing consists of calculating the desired voltages at every one of said ports; said processing to include functionality comprising an z-transform impedance matrix Z(z); and converting, using a digital-to-analog converter, the calculated desired voltages to output signal at every one of said ports.

[00128] The method of claim A3 where: said functionality comprises any difference equation relating desired port current i[n] to digitized port voltage v[n], when the sampling period is T for both the digital-to-analog converter and the analog-to-digital converter.

[00129] The method of claim A10 where: said functionality comprises any difference equation relating desired port voltage v[n] to digitized port voltage i[n], when the sampling period is T for both the digital-to-analog converter and the analog-to-digital converter.

[00130] The method of claim A17 where: said functionality comprises any desired z-transform admittance matrix Y(z).

[00131] The method of claim A19 where: said functionality comprises any desired z-transform impedance matrix Z(z).

[00132] The method of claim A17 where: said functionality includes an adaptive method for determining the initial external impedance Ze(s) seen by one or more ports by first generating a current impulse using said digital-to-analog converters, measuring the impulse response current using said analog-to-digital converters, then computing desired processing functionality Y(z).

[00133] The method of claim A25 where: said functionality includes an adaptive method for determining the external impedance Ze(s) seen by the port by using a pseudorandom current instead of said current impulse.

[00134] The method of claim A19 where: said functionality includes an adaptive method for determining the initial external impedance Ze(s) seen by one or more ports by first generating a voltage impulse using said digital-to-analog converters, measuring the impulse response current using said analog-to-digital converters, then computing desired processing functionality Z(z).

[00135] The method of claim A27 where: said functionality includes an adaptive method for determining the external impedance Ze(s) seen by the port by using a pseudorandom current instead of said current impulse.

[00136] The method of claim A1 where: said functionality comprises any difference equation relating desired port current i[n] to digitized port voltage v[n], when the sampling period is T for all of the digital-to-analog converters and the analog-to-digital converters.


The method of claim A1 where: said functionality includes an adaptive method for determining the initial external impedance Ze(s) seen by one or more ports by first generating a current or voltage impulse using said digital-to-analog converters, measuring the impulse response currents or voltages using said analog-to-digital converters, then computing desired processing functionality Y(z) or Z(z).

The method of claim A32 where: said functionality includes an adaptive method for determining the external impedance Ze(s) seen by the port by using a pseudorandom current instead of said current impulse.

The method of claim A2 where: signals are forces, temperatures, pressures, velocity, position, torque, or flow rate.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of embodiments of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to embodiments of the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of embodiments of the invention. The embodiment was chosen and described in order to best explain the principles of embodiments of the invention and the practical application, and to enable others of ordinary skill in the art to understand embodiments of the invention for various embodiments with various modifications as are suited to the particular use contemplated.

Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art appreciate that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown and that embodiments of the invention have other applications in other environments. This application is intended to cover any adaptations or variations of the present invention. The following claims are in no way intended to limit the scope of embodiments of the invention to the specific embodiments described herein.
CLAIMS

What is claimed is:

1. A method to implement circuits and circuit elements having one or more ports, comprising:
   - digitizing, using analog-to-digital converters, continuous-time input signals received from one or more
     ports of a circuit to form discrete-time input signals;
   - receiving, at a digital signal processor, the discrete-time input signals and processing the discrete-time
     input signals to calculate a desired discrete-time output signals;
   - converting, using digital-to-analog converters, the calculated desired discrete-time output signal to form
     outputs of continuous-time output signals at the one or more ports of the circuit;
   - outputting the continuous-time output signals to the same one or more ports that receive the
     continuous-time input signals; and
   - producing, thereby, a desired relationship between the continuous-time output signals and the
     continuous-time input signals at the one or more ports.

2. The method of claim 1, wherein the digital signal processor performs processing having functionality of
   at least one of convolution, difference equations, admittance matrices, impedance matrices, nonlinearity,
   adaptive control, adaptive stabilization, and time-variance.

3. The method of claim 2 wherein:
   - said digitizing comprises digitizing the continuous-time input voltage at the port of a component having
     only one port to form discrete-time input signal \( v[n] \);
   - said processing comprises calculating the desired discrete-time output signal \( i[n] \) that determines
     current for the one port;
   - said processing to include functionality comprising convolution or difference equations;
   - and
   - said converting comprises converting the discrete-time output signal \( i[n] \) to form a continuous-time
     output signal current - at said one port. 

4. The method of claim 3 where:
   - said functionality comprises at least one of:
     - a difference equation \( i[n] = C (v[n] - v[n-1])/T \) for a preferentially negative capacitance \( C \),
       relating desired discrete-time output signal port current \( i[n] \) to digitized discrete-time input signal port voltage \( v[n] \),
       when the sampling period is \( T \) for both the digital-to-analog converter and the analog-to-digital converter;
     - a difference equation \( i[n] = i[n-1] + T v[n]/L \) for a preferentially negative inductance \( L \), relating
       desired discrete-time output signal port current \( i[n] \) to digitized discrete-time input signal port voltage \( v[n] \),
       when the sampling period is \( T \) for both the digital-to-analog converter and the analog-to-digital converter;
     - a convolution relating desired discrete-time output signal port current \( i[n] \) to digitized discrete-time
       input signal port voltage \( v[n] \), where \( i[n] = v[n] * h[n] \), with \( * \) denoting convolution, where impulse response \( h[n] \)
has z-transform $H(z)$, and where $H(z) = 2C (z - 1)/(z + 1)T$ for a preferentially negative capacitance $C$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter;

a convolution relating desired discrete-time output signal port current $i[n]$ to digitized discrete-time input signal port voltage $v[n]$, where $i[n]$ is $v[n] * h[n]$ with * denoting convolution, where impulse response $h[n]$ has z-transform $H(z)$, and where $H(z) = T(z + 1)/(2L (z - 1))$ for a preferentially negative inductance $L$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter;

an adaptive method for determining the initial external impedance $Z_e(s)$ seen by the port by first generating a current impulse using said digital-to-analog converter, measuring the impulse response voltage using said analog-to-digital converter, taking $Z_e(s) = \sum v(nT)e^{-ns}$, then computing desired processing functionality $H(z) = \{(Z_e(s) - Z_i(s))/(Z_e(s)Z_i(s))\}_i[s=(z-1)/(z+1)]$, where $Z_i(s)$ is the desired total impedance at the port.

5. The method of claim 4 where:

said functionality includes an adaptive method for determining the external impedance $Z_e(s)$ seen by the port by using a pseudorandom current instead of said current impulse.

6. The method of claim 2 where:

said digitizing consists of digitizing the continuous-time input current at the port of a component having only one port to form discrete-time input signal $i[n]$;

said processing consists of calculating the desired discrete-time output signal $v[n]$ that determines voltage at said one port;

said processing to include functionality comprising convolution or difference equations;

and

said converting, comprises converting the discrete-time output signal $v[n]$ to form a continuous-time output signal voltage at said one port.

7. The method of claim 6 wherein said functionality comprises one of:

- a difference equation $v[n] = L ((i[n] - i[n-1] + T i[n])/C$ for a preferentially negative inductance $L$, relating desired discrete-time output signal port voltage $v[n]$ to digitized discrete-time input signal port current $i[n]$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter.

- a difference equation $v[n] = v[n-1] + T i[n]$/C$ for a preferentially negative capacitance $C$, relating desired discrete-time output signal port voltage $v[n]$ to digitized discrete-time input signal port current $i[n]$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter;

- a convolution relating desired discrete-time output signal port voltage $v[n]$ to digitized discrete-time input signal port current $i[n]$, where $v[n] = [i[n] * h[n]]$ with * denoting convolution, where impulse response $h[n]$ has z-transform $H(z)$, and where $H(z) = 2L (z - 1)/(z + 1)T$ for a preferentially negative inductance $L$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter;

- a convolution relating desired discrete-time output signal port voltage $v[n]$ to digitized discrete-time input signal port current $i[n]$, where $v[n] = [i[n] * h[n]]$ with * denoting convolution, where impulse response $h[n]$ has z-transform $H(z)$, and where $H(z) = T (z + 1)/(2C (z - 1))$ for a preferentially negative capacitance $C$, when the sampling period is $T$ for both the digital-to-analog converter and the analog-to-digital converter; and
an adaptive method for determining the initial external impedance $Z_d(s)$ seen by the port by first
generating a voltage impulse using said digital-to-analog converter, measuring the impulse response current
using said analog-to-digital converter, then computing desired processing functionality $H(z)$.

8. The method of claim 2 where:
said digitizing consists of digitizing the continuous-time input voltages at every port of a circuit to form
discrete-time input signals wherein the at least one or more ports comprises at least two or more ports;
said processing consists of calculating the desired discrete-time output signals that determine currents
at every one of said two or more ports;
said processing to include functionality comprising an $z$-transform admittance matrix $Y(z)$; and
said converting, comprises converting the discrete-time output signals to form a continuous-time output
signal currents at every one of said two or more ports.

9. The method of claim 2 where:
said digitizing consists of digitizing the continuous-time input currents at every port of the circuit to form
discrete-time input signals wherein the one or more ports comprises two or more ports;
said processing consists of calculating the desired discrete-time output signals that determine voltages
at every one of said two or more ports;
said processing to include functionality comprising a $z$-transform impedance matrix $Z(z)$; and
said converting, comprises converting the discrete-time output signals to form a continuous-time output
signal voltages at every one of said two or more ports.

10. The method of claim 8 where:
said functionality comprises any difference equation relating desired discrete-time output currents $i[n]$ to
digitized discrete-time input voltages $v[n]$, when the sampling period is $T$ for both the digital-to-analog converter
and the analog-to-digital converter.

11. The method of claim 8 where:
said functionality comprises one of: any desired $z$-transform admittance matrix $Y(z)$ and any desired $z$-
transform impedance matrix $Z(z)$.

12. The method of claim 11 where:
said functionality includes an adaptive method for determining the initial external impedance $Z_d(s)$ seen
by one or more ports by first generating a current impulse using said digital-to-analog converters, measuring the
impulse response current using said analog-to-digital converters, then computing desired processing functionality
$Y(z)$.

13. The method of claim 8 where:
said functionality comprises at least one of:

- a $z$-transform admittance matrix $Y(z)$ with
\[
Y(z) = \begin{bmatrix}
\frac{C}{T} (1 - z^{-1}) & -\frac{C}{T} (1 - z^{-1}) \\
-\frac{C}{T} (1 - z^{-1}) & -\frac{C}{T} (1 - z^{-1})
\end{bmatrix}
\]

for a preferentially negative capacitance \(C\), when the sampling period is \(T\) for all of the digital-to-analog converters and the analog-to-digital converters.

A z-transform admittance matrix \(Y(z)\) with

\[
Y(z) = \begin{bmatrix}
\frac{2C(z - 1)}{T(z + 1)} & \frac{2C(z - 1)}{T(z + 1)} \\
\frac{2C(z - 1)}{T(z + 1)} & \frac{2C(z - 1)}{T(z + 1)}
\end{bmatrix}
\]

for a preferentially negative capacitance \(C\), when the sampling period is \(T\) for all of the digital-to-analog converters and the analog-to-digital converters.

14. The method of claim 2 where:

said functionality includes an adaptive method for determining the initial external impedance \(Z_0(s)\) seen by one or more ports by first generating a voltage impulse using said digital-to-analog converters, measuring the impulse response current using said analog-to-digital converters, then computing desired processing functionality \(Z(z)\).

15. The method of claim 14 where:

said functionality includes an adaptive method for determining the external impedance \(Z_e(s)\) seen by the port by using a pseudorandom current instead of said current impulse.

16. The method of claim 2 where:

said functionality comprises at least one of:

- any desired z-transform admittance matrix \(Y(z)\),
- any desired z-transform impedance matrix \(Z(z)\),
- any difference equation relating desired port current \(i[n]\) to digitized port voltage \(v[n]\), when the sampling period is \(T\) for all of the digital-to-analog converters and the analog-to-digital converters.

17. The method of claim 9 where:

said functionality comprises at least one of:

- a z-transform impedance matrix \(Z(z)\) with

\[
Z(z) = \begin{bmatrix}
\frac{L}{T} (1 - z^{-1}) & -\frac{L}{T} (1 - z^{-1}) \\
-\frac{L}{T} (1 - z^{-1}) & -\frac{L}{T} (1 - z^{-1})
\end{bmatrix}
\]

for a preferentially negative inductance \(L\), when the sampling period is \(T\) for all of the digital-to-analog converters and the analog-to-digital converters.

- a z-transform impedance matrix \(Z(z)\) with
\[
Z(z) = \begin{bmatrix}
\frac{2L(z - 1)}{T(z + 1)} & \frac{2L(z - 1)}{T(z + 1)} \\
\frac{2L(z - 1)}{T(z + 1)} & \frac{2L(z - 1)}{T(z + 1)}
\end{bmatrix}
\]

for a preferentially negative inductance L, when the sampling period is T for all of the digital-to-analog converters and the analog-to-digital converters.

18. The method of claim 2 where:
said functionality includes an adaptive method for determining the initial external impedance \(Z_0(s)\) seen by one or more ports by first generating a current or voltage impulse using said digital-to-analog converters, measuring the impulse response currents or voltages using said analog-to-digital converters, then computing desired processing functionality \(Y(z)\) or \(Z(z)\).

19. The method of claim 1 wherein:
at least one of the signals comprises forces, temperatures, pressures, velocity, position, torque, or flow rate.

20. An apparatus to implement circuits and circuit elements having one or more ports, comprising:
analog-to-digital converters at every port to convert continuous-time input signals received from each port of a circuit into corresponding discrete-time input signals;
a digital signal processor to process and compute desired discrete-time output signals for each port from the said discrete-time input signals;
digital-to-analog converters at each port to convert the desired discrete-time output signals to continuous-time output signals at each port; and
outputs of said digital-to-analog converters connected to the inputs of said analog-to-digital converters at every port; and
where said continuous time output signals are currents when said continuous-time input signals are voltages, and where said continuous time output signals are voltages when said continuous-time input signals are currents.
FIGURE 9
A CONTINUOUS-TIME INPUT SIGNAL(S) (E.G., VOLTAGE, CURRENT, FORCE, TEMPERATURE, OR PRESSURE) IS DIGITIZED AT ONE OR MORE PORTS BY A DEVICE (E.G., ANALOG-TO-DIGITAL CONVERTERS OR ANALOG SAMPLERS) TO FORM A SAMPLED DISCRETE-TIME INPUT SIGNAL(S) OR VECTOR(S) (SUCH SAMPLING CAN BE SPATIAL, TEMPORAL, OR SPATIOTEMPORAL SAMPLING);

THE SAMPLED DISCRETE-TIME INPUT SIGNAL(S) IS PROCESSED BY A DIGITAL SIGNAL PROCESSOR (DSP) (E.G., DIGITAL LOGIC, ANALOG COMPUTERS, DIGITAL COMPUTERS, ETC.) TO CALCULATE A DISCRETE-TIME OUTPUT SIGNAL(S); PROCESSING OCCURS BY THE DSP (E.G., CONVOLUTION, ADMITTANCE MATRICES, IMPEDANCE MATRICES, NONLINEARITY, ADAPTIVE BEHAVIOR, TIME-VARIANCE AS DESIRED ETC.);

THE CALCULATED DISCRETE-TIME OUTPUT SIGNAL FROM THE DSP IS INPUTTED INTO A DIGITAL-TO-ANALOG CONVERTER AND IS CONVERTED TO A DESIRED CONTINUOUS-TIME OUTPUT SIGNAL (E.G., CURRENTS OR VOLTAGES) AT SAID ONE OR MORE PORTS BY MEANS SUCH AS DIGITAL-TO-ANALOG CONVERTERS;

THE ONE OR MORE PORTS WHERE THE INPUT SIGNAL(S) IS RECEIVED RECEIVES THE DESIRED CONTINUOUS-TIME OUTPUTTED SIGNAL(S)

FIGURE 20
AN OBSERVED CONTINUOUS-TIME INPUT SIGNAL V(T) AT A PORT IS DIGITIZED BY MEANS OF A VOLTAGE-INPUT ANALOG-TO-DIGITAL CONVERTER TO FORM A SAMPLED DISCRETE-TIME INPUT SIGNAL V[N], WHERE V[N]=V(NT) FOR SAMPLING PERIOD T, AND WHERE SAID ANALOG-TO-DIGITAL CONVERTER MAY HAVE A HIGH INPUT IMPEDANCE;

SAID SAMPLED DISCRETE-TIME INPUT SIGNAL V[N], IS PROCESSED BY DIGITAL SIGNAL PROCESSOR MEANS (E.G., DIGITAL LOGIC, ANALOG COMPUTERS, OR DIGITAL COMPUTERS TO CALCULATE A DESIRED DISCRETE-TIME OUTPUT SIGNAL I[N] AT SAID PORT;


SAID CALCULATED DESIRED DISCRETE-TIME OUTPUT SIGNAL I[N] IS CONVERTED TO CONTINUOUS-TIME OUTPUT SIGNAL CURRENT I(T) AT SAID ONE OR MORE PORTS OF THE BY A CURRENT-OUTPUT DIGITAL-TO-ANALOG CONVERTER WITH SAMPLING PERIOD T, WHERE SAID DIGITAL-TO-ANALOG CONVERTER PREFERENTIALLY HAS HIGH OUTPUT IMPEDANCE.

FIGURE 21
AN OBSERVED CONTINUOUS-TIME INPUT SIGNAL CURRENT \( i(t) \) AT A PORT IS DIGITIZED BY A CURRENT-INPUT ANALOG-TO-DIGITAL CONVERTER TO FORM A SAMPLED DISCRETE-TIME INPUT SIGNAL \( i[n] \), WHERE \( i[n] = i(nt) \) FOR SAMPLING PERIOD \( T \), AND WHERE SAID ANALOG-TO-DIGITAL CONVERTER MAY HAVE LOW INPUT IMPEDANCE;

SAID SAMPLED DISCRETE-TIME INPUT SIGNAL \( i[n] \), IS PROCESSED BY MEANS (E.G., DIGITAL SIGNAL PROCESSORS, DIGITAL LOGIC, ANALOG COMPUTERS, OR DIGITAL COMPUTERS) TO CALCULATE A DESIRED DISCRETE-TIME OUTPUT SIGNAL \( v[n] \) AT SAID PORT;

SAID PROCESSING TO BE A DISCRETE-TIME CONVOLUTION WHERE DESIRED DISCRETE-TIME OUTPUT SIGNAL \( v[n] = i[n] \ast h[n] \) (WITH \( \ast \) DENOTING CONVOLUTION), HAVING IMPULSE RESPONSE \( h[n] \) WITH Z-TRANSFORM \( H(z) \) AND CORRESPONDING DIFFERENCE EQUATION REPRESENTATIONS, SUCH AS \( v[n] = l (i[n] - i[n-1])/T \) FOR A POSITIVE OR NEGATIVE INDUCTANCE \( L \);

SAID CALCULATED DESIRED DISCRETE-TIME OUTPUT SIGNAL \( v[n] \) TO BE CONVERTED TO THE CONTINUOUS-TIME OUTPUT SIGNAL VOLTAGE \( v(t) \) AT SAID PORT BY MEANS OF A VOLTAGE-OUTPUT DIGITAL-TO-ANALOG CONVERTER WITH SAMPLING PERIOD \( T \), WHERE SAID DIGITAL-TO-ANALOG CONVERTER PREFERENTIALLY HAS LOW OUTPUT IMPEDANCE.

FIGURE 22
AN OBSERVED CONTINUOUS-TIME INPUT SIGNAL VECTOR V(T) IS DIGITIZED AT TWO OR MORE PORTS BY MEANS OF VOLTAGE-INPUT ANALOG-TO-DIGITAL CONVERTERS AT EVERY PORT TO FORM A SAMPLED DISCRETE-TIME INPUT SIGNAL VECTOR V[N], WHERE V[N]=V(NT) FOR SAMPLING PERIOD T, AND WHERE SAID ANALOG-TO-DIGITAL CONVERTERS MAY HAVE HIGH INPUT IMPEDANCES;

SAID SAMPLED DISCRETE-TIME INPUT SIGNAL VECTOR V[N], IS PROCESSED BY MEANS SUCH AS DIGITAL SIGNAL PROCESSORS, DIGITAL LOGIC, ANALOG COMPUTERS, OR DIGITAL COMPUTERS TO CALCULATE A DESIRED CURRENT DISCRETE-TIME OUTPUT SIGNAL VECTOR I[N] AT SAID PORTS;

SAID PROCESSING TO BE A DISCRETE-TIME CONVOLUTION WHERE THE Z-TRANSFORM OF THE DESIRED DISCRETE-TIME OUTPUT VECTOR IS DETERMINED FROM I(Z)=V(Z)Y(Z) AND WHERE THE DESIRED RESPONSE IS DETERMINED BY Z-TRANSFORM ADMITTANCE MATRIX Y(Z), AND WHERE I(Z) AND V(Z) ARE THE Z-TRANSFORMS OF VECTORS I[N] AND V[N] RESPECTIVELY;

SAID CALCULATED DESIRED DISCRETE-TIME OUTPUT SIGNAL VECTOR I[N] TO BE CONVERTED TO THE CONTINUOUS-TIME OUTPUT SIGNAL VECTOR CURRENT I(T) AT SAID PORTS BY MEANS OF CURRENT-OUTPUT DIGITAL-TO-ANALOG CONVERTERS AT EVERY PORT WITH SAMPLING PERIOD T, WHERE SAID DIGITAL-TO-ANALOG CONVERTERS PREFERENTIALLY HAVE HIGH OUTPUT IMPEDANCES.

FIGURE 23
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H03M 1/00 (2015.01)
CPC - H03M 1/00 (2015.04)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - G06F 19/00; H03M 1/00 (2015.01)
USPC - 34/11/10, 144, 155

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
CPC - H03M 1/00; H03M 3/464 (2015.04) (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, Google Patents, Google Scholar.
Search terms used: Analog to digital, digital to analog, impulse response, feedback, non-foster, voltage, current, converter, input, output

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<td>3, 6, 8-11, 16, 20</td>
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<td>4-5, 7, 12-15 and 17-18</td>
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<td>8-11, 16</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:
  "A" document defining the general state of the art which is not considered to be of particular relevance
  "E" earlier application or patent but published on or after the international filing date
  "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
  "O" document referring to an oral disclosure, use, exhibition or other means
  "P" document published prior to the international filing date but later than the priority date claimed
  "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
  "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of mailing of the international search report 23 JUL 2015

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