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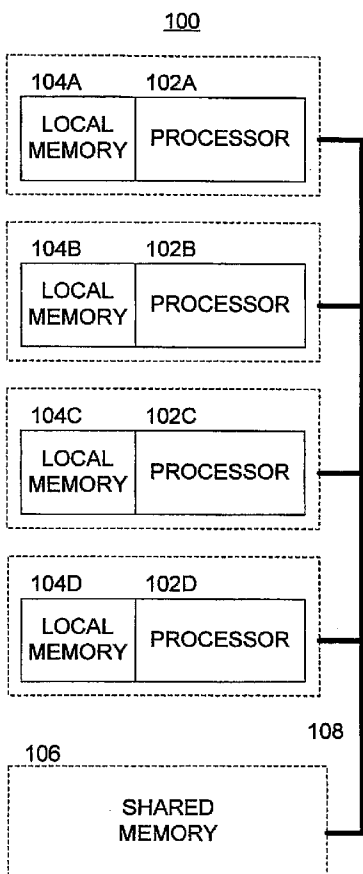
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- (54) Title: **METHODS AND APPARATUS FOR INSTRUCTION SET EMULATION**
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(57) Abstract: Methods and apparatus provide for translating a software program page by page from a first instruction set architecture (ISA) into a second ISA using one or more of a set of processors of a multi-processor system; and executing the translated software program using a dedicated other processor of the multi-processor system.



ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,
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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GROSS THOMAS ; ZOBEL ANGELIKA ; ZOLG MARKUS: "Parallel compilation for a parallel machine" PROCEEDINGS OF THE SIGPLAN '89 CONFERENCE ON PROGRAMMING LANGUAGE DESIGN AND IMPLEMENTATION, [Online] 21 June 1989 (1989-06-21), pages 91-100, XP002394370 Portland, OR, USA ISSN: 0362-1340 Retrieved from the Internet: URL: http://delivery.acm.org/10.1145/80000/74826/p91-gross.pdf?key1=74826&key2=2803215511&coll=ACM&d1=ACM&CFID=15151515&CFTOKEN=6184618 [retrieved on 2006-08-08] abstract; figures 1,2 <div style="text-align: center; margin-top: 10px;">----- -/--</div>	1-27

Further documents are listed in the continuation of Box C. See patent family annex.

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CAIN H W ET AL: "A dynamic binary translation approach to architectural simulation" COMPUTER ARCHITECTURE NEWS, ACM, NEW YORK, NY, US, vol. 29, no. 1, March 2001 (2001-03), pages 27-36, XP002237506 ISSN: 0163-5964 abstract	1-27
A	----- COGSWELL B H ET AL: "Timing insensitive binary-to-binary migration across multiprocessor architectures" PARALLEL AND DISTRIBUTED REAL-TIME SYSTEMS, 1995. PROCEEDINGS OF THE THIRD WORKSHOP ON SANTA BARBARA, CA, USA 25 APRIL 1995, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, 1995, pages 193-194, XP010148075 ISBN: 0-8186-7099-1 abstract -----	1-27