

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
17 August 2006 (17.08.2006)

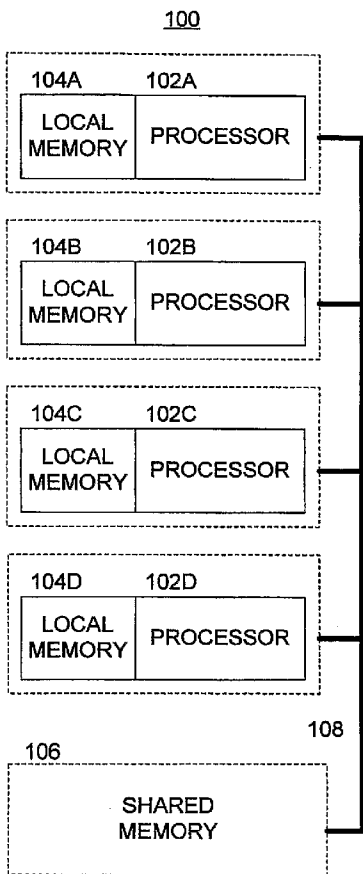
PCT

(10) International Publication Number
WO 2006/085639 A3

- (51) International Patent Classification:
G06F 9/45 (2006.01) *G06F 9/46* (2006.01)
- (21) International Application Number:
PCT/JP2006/302422
- (22) International Filing Date: 7 February 2006 (07.02.2006)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
11/053,512 8 February 2005 (08.02.2005) US
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- (54) Title: **METHODS AND APPARATUS FOR INSTRUCTION SET EMULATION**
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,

[Continued on next page]

WO 2006/085639 A3



(57) Abstract: Methods and apparatus provide for translating a software program page by page from a first instruction set architecture (ISA) into a second ISA using one or more of a set of processors of a multi-processor system; and executing the translated software program using a dedicated other processor of the multi-processor system.



ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,
RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA,
GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

(88) Date of publication of the international search report:
8 February 2007

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

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| International application No PCT/JP2006/302422 |
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A. CLASSIFICATION OF SUBJECT MATTER
 INV. G06F9/45 G06F9/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|---|-----------------------|
| X | GROSS THOMAS ; ZOBEL ANGELIKA ; ZOLG MARKUS: "Parallel compilation for a parallel machine" PROCEEDINGS OF THE SIGPLAN '89 CONFERENCE ON PROGRAMMING LANGUAGE DESIGN AND IMPLEMENTATION, [Online] 21 June 1989 (1989-06-21), pages 91-100, XP002394370 Portland, OR, USA ISSN: 0362-1340 Retrieved from the Internet: URL: http://delivery.acm.org/10.1145/80000/74826/p91-gross.pdf?key1=74826&key2=2803215511&coll=ACM&d1=ACM&CFID=15151515&CFTOKEN=6184618 [retrieved on 2006-08-08] abstract; figures 1,2 <div style="text-align: center; margin-top: 10px;">----- -/--</div> | 1-27 |

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| Date of the actual completion of the international search 11 August 2006 | Date of mailing of the international search report 30/08/2006 |
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| Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016 | Authorized officer Müller, T |
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INTERNATIONAL SEARCH REPORT

International application No

PCT/JP2006/302422

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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| A | CAIN H W ET AL: "A dynamic binary translation approach to architectural simulation" COMPUTER ARCHITECTURE NEWS, ACM, NEW YORK, NY, US, vol. 29, no. 1, March 2001 (2001-03), pages 27-36, XP002237506 ISSN: 0163-5964 abstract | 1-27 |
| A | ----- COGSWELL B H ET AL: "Timing insensitive binary-to-binary migration across multiprocessor architectures" PARALLEL AND DISTRIBUTED REAL-TIME SYSTEMS, 1995. PROCEEDINGS OF THE THIRD WORKSHOP ON SANTA BARBARA, CA, USA 25 APRIL 1995, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, 1995, pages 193-194, XP010148075 ISBN: 0-8186-7099-1 abstract ----- | 1-27 |