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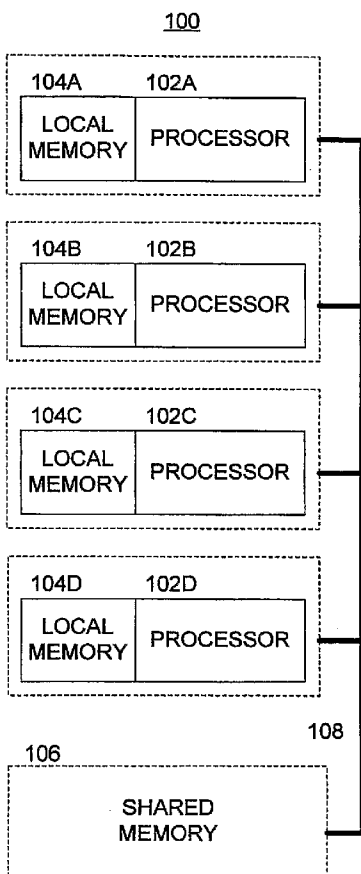
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- (71) Applicant (for all designated States except US): **SONY COMPUTER ENTERTAINMENT INC.** [JP/JP];
2-6-21, Minami-Aoyama, Minato-ku, Tokyo, 1070062 (JP).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): **SUZUOKI,**
- (54) Title: METHODS AND APPARATUS FOR INSTRUCTION SET EMULATION
- (55) Masakazu [JP/JP]; c/o SONY COMPUTER ENTERTAINMENT INC., 2-6-21, Minami-Aoyama, Minato-ku, Tokyo, 1070062 (JP).
- (74) Agent: **SUZUKI, Seigoh;** Pacific City Shiba Bldg., 6th Floor, 29-10, Shiba 2-chome, Minato-ku, Tokyo, 105-0014 (JP).
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(57) Abstract: Methods and apparatus provide for translating a software program page by page from a first instruction set architecture (ISA) into a second ISA using one or more of a set of processors of a multi-processor system; and executing the translated software program using a dedicated other processor of the multi-processor system.

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ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,
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INTERNATIONAL SEARCH REPORT

International application No PCT/JP2006/302422

A. CLASSIFICATION OF SUBJECT MATTER
 INV. G06F9/45 G06F9/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GROSS THOMAS ; ZOBEL ANGELIKA ; ZOLG MARKUS: "Parallel compilation for a parallel machine" PROCEEDINGS OF THE SIGPLAN '89 CONFERENCE ON PROGRAMMING LANGUAGE DESIGN AND IMPLEMENTATION, [Online] 21 June 1989 (1989-06-21), pages 91-100, XP002394370 Portland, OR, USA ISSN: 0362-1340 Retrieved from the Internet: URL: http://delivery.acm.org/10.1145/80000/74826/p91-gross.pdf?key1=74826&key2=2803215511&coll=ACM&d1=ACM&CFID=15151515&CFTOKEN=6184618 [retrieved on 2006-08-08] abstract; figures 1,2 <div style="text-align: center; margin-top: 10px;">----- -/--</div>	1-27

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- * Special categories of cited documents :
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| <p>*A* document defining the general state of the art which is not considered to be of particular relevance</p> <p>*E* earlier document but published on or after the international filing date</p> <p>*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>*O* document referring to an oral disclosure, use, exhibition or other means</p> <p>*P* document published prior to the international filing date but later than the priority date claimed</p> | <p>*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>*Z* document member of the same patent family</p> |
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Date of the actual completion of the international search 11 August 2006	Date of mailing of the international search report 30/08/2006
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer <div style="text-align: center; font-size: 1.2em;">Müller, T</div>
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INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CAIN H W ET AL: "A dynamic binary translation approach to architectural simulation" COMPUTER ARCHITECTURE NEWS, ACM, NEW YORK, NY, US, vol. 29, no. 1, March 2001 (2001-03), pages 27-36, XP002237506 ISSN: 0163-5964 abstract	1-27
A	----- COGSWELL B H ET AL: "Timing insensitive binary-to-binary migration across multiprocessor architectures" PARALLEL AND DISTRIBUTED REAL-TIME SYSTEMS, 1995. PROCEEDINGS OF THE THIRD WORKSHOP ON SANTA BARBARA, CA, USA 25 APRIL 1995, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, 1995, pages 193-194, XP010148075 ISBN: 0-8186-7099-1 abstract -----	1-27