PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

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PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2019/056029	14.10.2019	30.11.2018

International Patent Classification (IPC) or both national classification and IPC
INV. H03L7/18 H03L7/22

Applicant
CIENA CORPORATION

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Fax: +31 70 340 - 3016	see form PCT/ISA/210	Aouichi, Mohamed Telephone No. +31 70 340-0

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2019/056029

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

   a. ☐ forming part of the international application as filed:

      ☐ in the form of an Annex C/ST.25 text file.

      ☐ on paper or in the form of an image file.

   b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

   c. ☐ furnished subsequent to the international filing date for the purposes of international search only:

      ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).

      ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	3-5, 7, 8, 11, 12, 14, 15
	No:	Claims	1, 2, 6, 9, 10, 13
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-15
Industrial applicability (IA)	Yes:	Claims	1-15
	No:	Claims	

2. Citations and explanations

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following documents:

D1 US 2007/152757 A1 (SRIDHARAN KARTIK M [US]) 5 July 2007 (2007-07-05)

D2 EP 1 397 772 A1 (ANALOG DEVICES INC [US]) 17 March 2004 (2004-03-17)

D3 WO 2010/056813 A1 (ANALOG DEVICES INC [US]; PALMER WYN [US]; GENTILE KENNY [US]) 20 May 2010 (2010-05-20)

D4 US 8 493 111 B1 (BRADLEY DONALD ANTHONY [US]) 23 July 2013 (2013-07-23)

2 The present application does not meet the criteria of Article 33(2) PCT, because the subject-matter of claim 1 is not new.

D1 discloses (paragraph [0045] - paragraph [0051]; figures 5-7) a circuit (30) comprising:
a programmable frequency divider (328) which receives a high-speed clock (output of Multiply by N 326),fin, as an input and which provides a modulated reference clock (Output) as an output;
a Sigma-Delta modulator (320) which receives a Frequency Control Word (FCW) (321) and which is connected to the programmable frequency divider (328) to receive the modulated reference clock (20) as a sample clock (paragraph [0045]; figure 5) and to control an average frequency of the modulated reference clock (20); and
an integer-N Phase Lock Loop (PLL) (348; figure 7) which receives the modulated reference clock (Output) and outputs a clock output (output of the VCO 362).

3 The present application does not meet the criteria of Article 33(2) PCT, because the subject-matter of claim 1 is also not new with respect to D2 and D3, see cited passages in the Search Report.

4 The present application does not meet the criteria of Article 33(3) PCT, because the subject-matter of claim 1 does not involve an inventive step with respect to D4 taken alone, see passages cited in the Search Report.

5 The present application does not meet the criteria of Article 33(2) PCT, because the subject-matter of claim 9 is not new.

D1 discloses (paragraph [0045] - paragraph [0051]; figures 5-7) a method of operating a circuit comprising:
receiving a high-speed clock (output of Multiply by N 326),fin, as an input to a programmable frequency divider (328);
modulating the high-speed clock with a Sigma-Delta modulator (320) which is connected to the programmable frequency divider (328) to control an average frequency of an output of programmable frequency divider (328);
controlling the Sigma-Delta modulator (320,327) with a Frequency Control Word (FCW) (Fraction 321) and an integer divisor (Integer 329), each of the FCW (Fraction) and the integer divisor (Integer) is connected to the programmable frequency divider (328);
providing an output of the programmable frequency divider (328) as a modulated reference clock (Output), wherein the modulated reference clock (Output) is connected to the Sigma-Delta modulator (320,327) as a sample clock (paragraph [0045]; figure 5); and
receiving the modulated reference clock (Output) at an integer-N Phase Lock Loop (PLL) (348; Figure 7) and outputting a clock output (output of the VCO 326).

6 The present application does not meet the criteria of Article 33(2) PCT, because the subject-matter of claim 9 is also not new with respect to D2 and D3, see cited passages in the Search Report.

7 The present application does not meet the criteria of Article 33(3) PCT, because the subject-matter of claim 9 does not involve an inventive step with respect to D4 taken alone, see passages cited in the Search Report.

8 Dependent claims 2-8, 10-15 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step.

- The additional features of 3 and 11 concern a trivial implementation of the multiplier 326 of D1.

- The additional features of 6 and 13 concern trivial features of a sigma-delta modulator like that used in D1.

- The additional features of 5 and 12 concern are disclosed by D1 except for the fact that the circuit drives a Serializer/Deserializer which is obvious.

- The additional features of 4,7,8,14 and15 are obvious for the skilled person.

Re Item VIII

Certain observations on the international application

1 The application does not meet the requirements of Article 6 PCT, because claims 1-5,8,10,11 and 15 are not clear.

1.1 Some of the features in the apparatus claim 1 relate to a method of using the apparatus rather than clearly defining the apparatus in terms of its technical features. The intended limitations are therefore not clear from this claim, contrary to the requirements of Article 6 PCT.

The features concerned are the following:

"a programmable frequency divider (14) **which receives** a high-speed clock ..." (emphasis added)
"a Sigma-Delta modulator (320) **which receives** a Frequency Control Word ..." (emphasis added)

"an integer-N Phase Lock Loop (PLL) (22) **which receives** the modulated reference clock ..." (emphasis added)

1.2 The parameters *I* and *M* in claims 2 and 10 are not defined.

1.3 it is not clear whether said second PLL defined in claim 3 is included in said circuit or not.

1.4 it is not clear whether said Digital-Analog Converter defined in claim 4 is included in said circuit or not.

1.5 it is not clear whether said Serializer/Deserializer defined in claim 5 is included in said circuit or not.

1.6 it is not clear whether said second PLL defined in claim 8 is included in said circuit or not.

1.7 it is not clear whether said second PLL defined in claim 3 and said second PLL defined in claim 8 are the same or not.

1.8 it is not clear whether said second PLL defined in claim 11 and said second PLL defined in claim 15 are the same or not.