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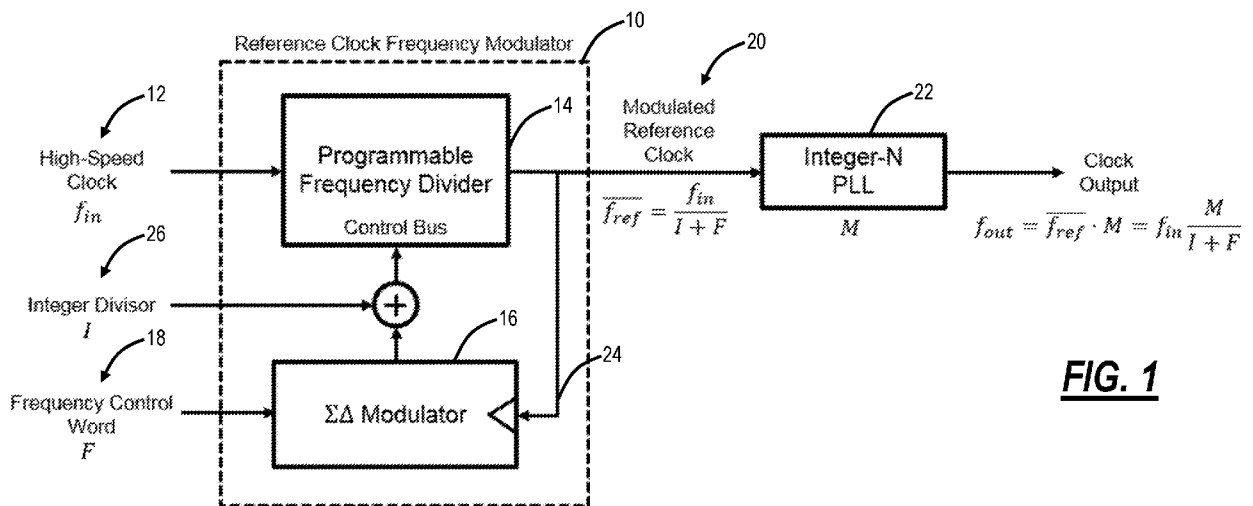


FIG. 1

(57) Abstract: A circuit (30) includes a programmable frequency divider (14) which receives a high-speed clock (12), f_{in} , as an input and which provides a modulated reference clock (20) as an output; a Sigma-Delta modulator (16) which receives a Frequency Control Word (FCW) (18) and which is connected to the programmable frequency divider (14) to receive the modulated reference clock (20) as a sample clock and to control an average frequency of the modulated reference clock (20); and an integer-N Phase Lock Loop (PLL) (22) which receives the modulated reference clock (20) and outputs a clock output..

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Fractional frequency synthesis by sigma-delta modulating frequency of a reference clock

FIELD OF THE DISCLOSURE

[0001] The present disclosure generally relates to electrical circuits. More particularly, the present disclosure relates to systems and methods for fractional frequency synthesis by sigma-delta modulating frequency of a reference clock such as to realize a Numerically Controlled Oscillator (NCO) function.

BACKGROUND OF THE DISCLOSURE

[0002] A Numerically Controlled Oscillator (NCO) is a digital signal generator which creates a synchronous, discrete-time, discrete-valued representation of a waveform. NCOs are used in many communications systems including digital up/down converters used in wireless and software radio systems, digital Phase Lock Loops (PLL), radar systems, drivers for optical or acoustic transmissions, and multilevel modulators/demodulators. The popular approach to fractional-N frequency synthesis using sigma-delta modulation utilizes a fully dedicated fractional-N Type-II PLL-based synthesizer (Phase-Frequency Detector (PFD), charge pump, loop filter, Voltage Controlled Oscillator (VCO), programmable frequency divider, and Sigma-Delta modulator in a feedback path, which uses a constant frequency clock as an input.

[0003] If an integer-N synthesizer is already available, it would require a redesign to convert it to a fractional-N synthesizer. Also, for realizing the NCO function serving as the reference clock of another PLL (e.g., a PLL in a Serialized/Deserializer (SerDes) system), a fully dedicated fractional PLL is required. These approaches require additional footprint, power, and cost. The dedicated PLL is an analog solution which is best verified in silicon, whereas a digital solution could be verified more easily. The frequency resolution of the sigma-delta modulated divider is also limited by the frequency of the VCO.

BRIEF SUMMARY OF THE DISCLOSURE

[0004] In an embodiment, a circuit includes a programmable frequency divider which receives a high-speed clock, f_m , as an input and which provides a modulated reference clock as an output; a Sigma-Delta modulator which receives a Frequency Control Word (FCW) and which is connected to the programmable frequency divider to receive the modulated reference

clock as a sample clock and to control an average frequency of the modulated reference clock; and an integer-N Phase Lock Loop (PLL) which receives the modulated reference clock and outputs a clock output. The modulated reference clock average frequency is equal to $\frac{f_{in}}{I+FCW}$ and wherein the clock output frequency is equal to $f_{in} \frac{M}{I+FCW}$. The high-speed clock can be from a second PLL associated with the circuit. The second Phase Lock Loop (PLL) can be for a Digital-Analog Converter (DAC) sampling clock. The circuit can further include an integer divisor (I) that is connected to the programmable frequency divisor, and provides a Numerically Controlled Oscillator (NCO) function based on selected values for the FCW, the integer divisor, and the integer-N PLL, and wherein the circuit drives a Serializer/Deserializer (SerDes). The FCW can define a numerator value for the programmable frequency divider, and a denominator value for the programmable frequency divider can be set by one of i) rail voltages for an analog Sigma-Delta modulator and ii) a number of accumulator bits for a digital Sigma-Delta modulator. The circuit can be disposed in an Application Specific Integrated Circuit (ASIC) on a Printed Circuit Board (PCB). The high-speed clock can be from a second PLL on the ASIC which receives an input reference clock from the PCB.

[0005] In another embodiment, an apparatus includes a Printed Circuit Board (PCB) with a reference clock; a circuit including: a Phase Lock Loop (PLL) which is served by the reference clock; a programmable frequency divider which receives a high-speed clock, f_{in} , as an input and provides a modulated reference clock as an output, wherein the high-speed clock is reused from the reference clock; a Sigma-Delta modulator which receives a Frequency Control Word (FCW), and which is connected to the programmable frequency divider to receive the modulated reference clock as a sample clock and to control an average frequency of the modulated reference clock; and an integer-N Phase Lock Loop (PLL) which receives the modulated reference clock and outputs a clock output. The modulated reference clock average frequency is equal to $\frac{f_{in}}{I+FCW}$, and wherein the clock output frequency is equal to $f_{in} \frac{M}{I+FCW}$. The high-speed clock can be from a second PLL associated with the circuit. The circuit can further include an integer divisor (I) that is connected to the programmable frequency divisor, and provides a Numerically Controlled Oscillator (NCO) function based on selected values for the FCW, the integer divisor, and the integer-N PLL, and wherein the circuit drives a Serializer/Deserializer (SerDes). The FCW can define a numerator value for the programmable frequency divider and a denominator value for the programmable frequency divider can be set

by one of i) rail voltages for an analog Sigma-Delta modulator and ii) a number of accumulator bits for a digital Sigma-Delta modulator.

[0006] In a further embodiment, a method of operating a circuit includes receiving a high-speed clock, f_{in} , as an input to a programmable frequency divider; modulating the high-speed clock with a Sigma-Delta modulator which is connected to the programmable frequency divider to control an average frequency of an output of programmable frequency divider; controlling the Sigma-Delta modulator with a Frequency Control Word (FCW) and an integer divisor, each of the FCW and the integer divisor is connected to the programmable frequency divider; providing an output of the programmable frequency divider as a modulated reference clock, wherein the modulated reference clock is connected to the Sigma-Delta modulator as a sample clock; and receiving the modulated reference clock at an integer-N Phase Lock Loop (PLL) and outputting a clock output. The modulated reference clock average frequency is equal to $\frac{f_{in}}{I+FCW}$, and wherein the clock output frequency is equal to $f_{in} \frac{M}{I+FCW}$. The high-speed clock can be from a second Phase Lock Loop (PLL) associated with the circuit. The circuit can provide a Numerically Controlled Oscillator (NCO) function based on selected values for the FCW, the integer divisor, and the integer-N PLLC, and wherein the circuit drives a Serializer/Deserializer (SerDes). The FCW can define a numerator value for the programmable frequency divider and a denominator value for the programmable frequency divider can be set by one of i) rail voltages for an analog Sigma-Delta modulator and ii) a number of accumulator bits for a digital Sigma-Delta modulator. The circuit can be disposed in an Application Specific Integrated Circuit (ASIC) on a Printed Circuit Board (PCB). The high-speed clock can be from a second PLL on the ASIC which receives an input reference clock from the PCB.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The present disclosure is illustrated and described herein with reference to the various drawings, in which like reference numbers are used to denote like system components/method steps, as appropriate, and in which:

[0008] FIG. 1 is a block diagram of a reference clock frequency modulator device that divides a high-speed clock by a programmable frequency divider controlled through a Sigma-Delta ($\Sigma\Delta$) modulator;

[0009] FIG. 2 is a graph of frequency versus time illustrating the simulated output frequency of the PLL settling to 13.9762 GHz; the desired multiple of the fractionally divided input clock frequency 14.3136 GHz, utilizing the reference clock frequency modulator device of FIG. 1;

[0010] FIG. 3 is a block diagram of an Application Specific Integrated Circuit (ASIC) on a Printed Circuit Board (PCB) with the ASIC including the reference clock frequency modulator device of FIG. 1 and a high-speed clock available as an input to the ASIC;

[0011] FIG. 4 is a diagram of the phase/frequency domain power spectral density at the various stages of the proposed NCO scheme via the reference clock frequency modulator device of FIG. 1; and

[0012] FIG. 5 is a flowchart of a process for operating a circuit.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0013] The present disclosure relates to systems and methods for fractional frequency synthesis by sigma-delta modulating frequency of a reference clock such as to realize a Numerically Controlled Oscillator (NCO) function. The systems and methods achieve fractional-N frequency synthesis using phase-locked loops (PLL). In an embodiment, the systems and methods provide an electrical circuit which can be placed as the reference clock input to an existing integer-N PLL-based frequency synthesizer for achieving fractional-N frequency synthesis without the need of a dedicated fractional-N PLL. The high-speed clock applied to the programmable frequency divider can be coming from an already existing PLL. For example, in a high-speed device such as an optical transceiver, the high-speed clock signal can be taken from the PLL generating the Digital-Analog Converter (DAC) sampling clock. In the configuration, the NCO function that drives a SerDes PLL and tracks the client side is realized by sigma-delta modulating the frequency of a divided down clock generated by the transmitter's main high-speed PLL. Typically, the NCO block includes a fully dedicated fractional PLL. In the proposed solution, this extra PLL is completely bypassed, and the SerDes PLL is used to act as the phase/frequency domain interpolation filter to extract the desired encoded clock frequency. Advantageously, the proposed solution can be used in a high-speed optical transceiver/modem circuit to reduce design effort, power consumption, chip footprint, and cost by replacing NCO circuitry which generates clocks for the SerDes.

[0014] FIG. 1 is a block diagram of a reference clock frequency modulator device 10 that divides a high-speed clock 12 by a programmable frequency divider 14 controlled through a Sigma-Delta ($\Sigma\Delta$) modulator 16. The reference clock frequency modulator device 10 is an electrical circuit and can be integrated with other circuits such as on a chip, Application Specific Integrated Circuit (ASIC), etc. The other circuits can include a SerDes and other circuits. The high-speed clock 12, f_{in} , can be an already available high-frequency clock on the chip, ASIC, SerDes, etc. For example, the high-speed clock 12 can be from an already existing PLL used to clock data converters. Various, the reference clock frequency modulator device 10 can be used to provide a Numerically Controlled Oscillator (NCO) function.

[0015] The high-speed clock 12 is connected to the programmable frequency divider 14 which is configured to divide the high-speed clock 12, and the programmable frequency divider 14 is controlled by the Sigma-Delta modulator 16. The Sigma-Delta modulator 16 is input with a Frequency Control Word (FCW) 18, F , which is used to control the average frequency of the output of the programmable frequency divider 14. A frequency output 20 serves as a modulated reference clock to a PLL based integer-N frequency synthesizer/PLL 22 as well as the sample clock 24 for the Sigma-Delta modulator 16. The integer-N frequency synthesizer/PLL 22 typically includes a Phase Frequency Detector (PFD), charge pump, loop filter, Voltage-Controlled Oscillator (VCO), and a frequency divider, however other variants of PLL-based integer-N frequency synthesizers can be used so long as the loop filter is present. The frequency output 20 is input as the reference clock to an available integer-N PLL based synthesizer to achieve fractional-N frequency synthesis.

[0016] Through the modulation of the reference clock 20, the integer-N PLL 22 can achieve fractional-N frequency synthesis. It is known that the loop dynamics of the integer-N PLL 22 effectively set the output frequency of a VCO to be the product of the reference clock 20 frequency and a divisor ratio M set by the frequency divider (integer-N PLL 22). Since the closed-loop transfer function of such a PLL has a low-pass characteristic in both the frequency and phase domain, the average frequency of the modulated reference clock $\overline{f_{ref}}$ multiplied by M is observed at the output of the integer-N PLL 22. The average frequency of the reference clock 20 is given by dividing the input high-speed clock 12 frequency by the summation of an integer divisor I 26 of the programmable frequency divider 14 and the fractional value F which the FCW 18 represents. The FCW 18 typically defines the numerator of the fractional value; a Direct Current (DC) voltage with the denominator set by the rail voltages if the Sigma-Delta modulator 16 is an analog circuit or a binary integer with the denominator set by the number

of accumulator bits if the Sigma-Delta modulator 16 is digital. Given an input clock frequency f_{in} , the output frequency f_{out} can be determined:

$$f_{out} = f_{in} \frac{M}{I + FCW}$$

[0017] For example, assume a digital Multi-stage noise shaping (MASH) 111 sigma-delta modulator with 14-bit accumulators is used, M is 40, and the desired output frequency is 13.9762 GHz. Suppose a 14.3136 GHz clock is available as an input clock, then I can be set to 40 and F can be set to about 0.9655 using a digital FCW with a binary integer value of 15819:

$$13.9762 \text{ GHz} \approx 14.3136 \text{ GHz} \frac{40}{40 + 15819/2^{14}}$$

[0018] FIG. 2 is a graph of frequency versus time illustrating the simulated output frequency of the PLL settling to 13.9762 GHz; the desired multiple of the fractionally divided input clock frequency 14.3136 GHz, utilizing the reference clock frequency modulator device 10.

[0019] FIG. 3 is a block diagram of an Application Specific Integrated Circuit (ASIC) 30 on a Printed Circuit Board (PCB) 32 with the ASIC 30 including the reference clock frequency modulator device 10 and the high-speed clock 12 available as an input to the ASIC 30. The high-speed clock 12 can be input from a reference clock 34 on the PCB 32 which is used to service DACs and/or Analog-Digital Converters (ADCs). The reference clock 34 can be connected to a DAC integer PLL 36 to provide the high-speed clock 12 to the reference clock frequency modulator device 10.

[0020] Again, the reference clock frequency modulator device 10 can receive the high-speed clock 12 which is from the reference clock 34, achieving fractional-N frequency synthesis without the need of a dedicated fractional-N PLL. The high-speed clock 12 applied to the programmable frequency divider 14 can be coming from an already existing PLL on the PCB 32. For example, the ASIC 30 and PCB 32 can be for a high-speed optical transceiver, and the high-speed clock 12 signal can be taken from the PLL generating the DAC sampling clock. In the configuration depicted in FIG. 3, the NCO function of the reference clock frequency modulator device 10 drives a SerDes PLL and tracks the client side is realized by

sigma-delta modulating the frequency of a divided down clock generated by the transmitter's main high-speed PLL. Typically, the NCO block includes a fully dedicated fractional PLL. In the present disclosure, this extra PLL is completely bypassed and relying on the SerDes PLL to act as the phase/frequency domain interpolation filter to extract the desired encoded clock frequency.

[0021] FIG. 4 is a diagram of the phase/frequency domain power spectral density 50, 52, 54, 56 at the various stages of the proposed NCO scheme via the reference clock frequency modulator device 10. With the present disclosure, the approach is to send a reference clock (denoted by the phase/frequency domain power spectral density 50) with the desired frequency being sigma-delta encoded (denoted by the phase/frequency domain power spectral density 52) to a Digital-to-Frequency Conversion (DFC) process 60 (denoted by the phase/frequency domain power spectral density 54) to the SerDes PLL (denoted by the phase/frequency domain power spectral density 56) which acts as a frequency domain filter to extract the desired "clean" reference as depicted in FIG. 4. In fact, the modulated output can be input as the reference clock to the integer-N synthesizer (e.g., the integer-N PLL 22), without any redesign required, to convert it to a fractional-N synthesizer. Since the present disclosure can be fully implemented using solely digital circuits, it benefits from an uncomplicated design that can be easily verified. The frequency of the high-speed clock 12 and the range of divisors used during operation by the programmable frequency divider can be selected to optimize jitter performance, whereas a dedicated PLL would be limited by the frequency of the VCO.

[0022] FIG. 5 is a flowchart of a process 80 for operating a circuit. The process 80 includes receiving a high-speed clock, f_{in} , as an input to a programmable frequency divider (step 81); modulating the high-speed clock with a Sigma-Delta modulator which is connected to the programmable frequency divider to control an average frequency of an output of programmable frequency divider (step 82); controlling the Sigma-Delta modulator with a Frequency Control Word (FCW), F , and an integer divisor, I , each of the FCW and the integer divisor is connected to the programmable frequency divider (step 83); providing an output of the programmable frequency divider as a modulated reference clock, wherein the modulated reference clock is connected to the Sigma-Delta modulator as a sample clock (step 84); and receiving the modulated reference clock at an integer-N Phase Lock Loop (PLL) and outputting a clock output (step 85).

[0023] The modulated reference clock is equal to $\frac{f_{in}}{I+F}$, and wherein the clock output is equal to equal to $f_{in} \frac{M}{I+F}$. The high-speed clock can be from an existing Phase Lock Loop (PLL) associated with the circuit. The circuit can provide a Numerically Controlled Oscillator (NCO) function based on selected values for the FCW, the integer divisor, and the integer-N PLLC, and wherein the circuit drives a Serializer/Deserializer (SerDes). The FCW defines a numerator value for the programmable frequency divider and a denominator value for the programmable frequency divider is set by one of i) rail voltages for an analog Sigma-Delta modulator and ii) a number of accumulator bits for a digital Sigma-Delta modulator. The circuit can be disposed in an Application Specific Integrated Circuit (ASIC) on a Printed Circuit Board (PCB). The high-speed clock can be from an existing PLL on the ASIC which receives an input reference clock from the PCB.

[0024] In another embodiment, a circuit includes a programmable frequency divider 14 which receives a high-speed clock 12, f_{in} , as an input; a Sigma-Delta modulator 16 which receives a Frequency Control Word (FCW) 18, F , and which is connected to the programmable frequency divider 14 to control an average frequency of an output of programmable frequency divider 14; an integer divisor 26, I , which is connected to the programmable frequency divider 14; an output of the programmable frequency divider which provides a modulated reference clock 20, wherein the modulated reference clock 20 is connected to the Sigma-Delta modulator 16 as a sample clock 24; and an integer-N Phase Lock Loop (PLL) 22 which receives the modulated reference clock 20 and outputs a clock output.

[0025] The modulated reference clock is equal to $\frac{f_{in}}{I+F}$, and wherein the clock output is equal to equal to $f_{in} \frac{M}{I+F}$. The high-speed clock can be from an existing Phase Lock Loop (PLL) associated with the circuit. The existing Phase Lock Loop (PLL) can be for a Digital-Analog Converter (DAC) sampling clock. The circuit can provide a Numerically Controlled Oscillator (NCO) function based on selected values for the FCW, the integer divisor, and the integer-N PLLC, and wherein the circuit drives a Serializer/Deserializer (SerDes).

[0026] The FCW defines a numerator value for the programmable frequency divider, and a denominator value for the programmable frequency divider is set by one of i) rail voltages for an analog Sigma-Delta modulator and ii) a number of accumulator bits for a digital Sigma-Delta modulator. The circuit can be disposed in an Application Specific Integrated Circuit

(ASIC) on a Printed Circuit Board (PCB). The high-speed clock can be from an existing PLL on the ASIC which receives an input reference clock from the PCB.

[0027] In a further embodiment, an apparatus includes a Printed Circuit Board (PCB) 32 with a reference clock 34; a circuit 30 including: a Phase Lock Loop (PLL) 36 which is served by the reference clock; a programmable frequency divider 14 which receives a high-speed clock 12, f_{in} , as an input, wherein the high-speed clock 12 is reused from the reference clock 34; a Sigma-Delta modulator 16 which receives a Frequency Control Word (FCW) 18, F , and which is connected to the programmable frequency divider 14 to control an average frequency of an output of programmable frequency divider 14; an integer divisor 26, I , which is connected to the programmable frequency divider 14; an output of the programmable frequency divider 14 which provides a modulated reference clock 20, wherein the modulated reference clock 20 is connected to the Sigma-Delta modulator 16 as a sample clock 24; and an integer-N Phase Lock Loop (PLL) 22 which receives the modulated reference clock 20 and outputs a clock output.

[0028] The modulated reference clock is equal to $\frac{f_{in}}{I+F}$, and wherein the clock output is equal to equal to $f_{in} \frac{M}{I+F}$. The existing Phase Lock Loop (PLL) can be for a Digital-Analog Converter (DAC) sampling clock. The circuit can provide a Numerically Controlled Oscillator (NCO) function based on selected values for the FCW, the integer divisor, and the integer-N PLLC, and wherein the circuit drives a Serializer/Deserializer (SerDes). The FCW can define a numerator value for the programmable frequency divider and a denominator value for the programmable frequency divider is set by one of i) rail voltages for an analog Sigma-Delta modulator and ii) a number of accumulator bits for a digital Sigma-Delta modulator.

[0029] It will be appreciated that some embodiments described herein may include one or more generic or specialized processors (“one or more processors”) such as microprocessors; Central Processing Units (CPUs); Digital Signal Processors (DSPs); customized processors such as Network Processors (NPs) or Network Processing Units (NPU), Graphics Processing Units (GPUs), or the like; Field Programmable Gate Arrays (FPGAs); and the like along with unique stored program instructions (including both software and firmware) for control thereof to implement, in conjunction with certain non-processor circuits, some, most, or all of the functions of the methods and/or systems described herein. Alternatively, some or all functions may be implemented by a state machine that has no stored program instructions, or in one or

more Application Specific Integrated Circuits (ASICs), in which each function or some combinations of certain of the functions are implemented as custom logic or circuitry. Of course, a combination of the aforementioned approaches may be used. For some of the embodiments described herein, a corresponding device in hardware and optionally with software, firmware, and a combination thereof can be referred to as “circuitry configured or adapted to,” “logic configured or adapted to,” etc. perform a set of operations, steps, methods, processes, algorithms, functions, techniques, etc. on digital and/or analog signals as described herein for the various embodiments.

[0030] Although the present disclosure has been illustrated and described herein with reference to preferred embodiments and specific examples thereof, it will be readily apparent to those of ordinary skill in the art that other embodiments and examples may perform similar functions and/or achieve like results. All such equivalent embodiments and examples are within the spirit and scope of the present disclosure, are contemplated thereby, and are intended to be covered by the following claims.

CLAIMS

What is claimed is:

1. A circuit (30) comprising:
 - a programmable frequency divider (14) which receives a high-speed clock (12), f_{in} , as an input and which provides a modulated reference clock (20) as an output;
 - a Sigma-Delta modulator (16) which receives a Frequency Control Word (FCW) (18) and which is connected to the programmable frequency divider (14) to receive the modulated reference clock (20) as a sample clock and to control an average frequency of the modulated reference clock (20); and
 - an integer-N Phase Lock Loop (PLL) (22) which receives the modulated reference clock (20) and outputs a clock output.
2. The circuit (30) as claimed in claim 1, wherein the modulated reference clock (20) average frequency is equal to $\frac{f_{in}}{I+FCW}$, and wherein the clock output frequency is equal to $f_{in} \frac{M}{I+FCW}$.
3. The circuit (30) as claimed in claims 1-2, wherein the high-speed clock (12) is from a second PLL (36) associated with the circuit (30).
4. The circuit (30) as claimed in claim 3, wherein the second Phase Lock Loop (PLL) (36) is for a Digital-Analog Converter (DAC) sampling clock.
5. The circuit (30) as claimed in claims 1-4, wherein the circuit (30) further comprises an integer divisor (I) (26) that is connected to the programmable frequency divisor (14), and provides a Numerically Controlled Oscillator (NCO) function based on selected values for the FCW (18), the integer divisor (26), and the integer-N PLL (22), and wherein the circuit (30) drives a Serializer/Deserializer (SerDes).
6. The circuit as claimed in claim 1, wherein the FCW (18) defines a numerator value for the programmable frequency divider (14), and a denominator value for the programmable

frequency divider (14) is set by one of i) rail voltages for an analog Sigma-Delta modulator and ii) a number of accumulator bits for a digital Sigma-Delta modulator.

7. The circuit as claimed in claim 1, wherein the circuit is disposed in an Application Specific Integrated Circuit (ASIC) on a Printed Circuit Board (PCB).

8. The circuit as claimed in claim 7, wherein the high-speed clock (12) is from a second PLL on the ASIC which receives an input reference clock from the PCB.

9. A method of operating a circuit (30) comprising:
receiving a high-speed clock (12), f_{in} , as an input to a programmable frequency divider (14);

modulating the high-speed clock (12) with a Sigma-Delta modulator (16) which is connected to the programmable frequency divider (14) to control an average frequency of an output of programmable frequency divider (14);

controlling the Sigma-Delta modulator (16) with a Frequency Control Word (FCW) (18) and an integer divisor, each of the FCW (18) and the integer divisor is connected to the programmable frequency divider (14);

providing an output of the programmable frequency divider (14) as a modulated reference clock (20), wherein the modulated reference clock (20) is connected to the Sigma-Delta modulator (16) as a sample clock; and

receiving the modulated reference clock (20) at an integer-N Phase Lock Loop (PLL) (22) and outputting a clock output.

10. The method as claimed in claim 9, wherein the modulated reference clock average (20) frequency is equal to $\frac{f_{in}}{I+FCW}$, and wherein the clock output frequency is equal to $f_{in} \frac{M}{I+FCW}$.

11. The method as claimed in claims 9-10, wherein the high-speed clock is from a second Phase Lock Loop (PLL) (36) associated with the circuit (30).

12. The method as claimed in claims 9-11, wherein the circuit provides a Numerically Controlled Oscillator (NCO) function based on selected values for the FCW (18), the integer

divisor, and the integer-N PLLC (22), and wherein the circuit (30) drives a Serializer/Deserializer (SerDes).

13. The method as claimed in claims 9-12, wherein the FCW (18) defines a numerator value for the programmable frequency divider (14) and a denominator value for the programmable frequency divider (18) is set by one of i) rail voltages for an analog Sigma-Delta modulator and ii) a number of accumulator bits for a digital Sigma-Delta modulator.

14. The method as claimed in claims 9-13, wherein the circuit is disposed in an Application Specific Integrated Circuit (ASIC) on a Printed Circuit Board (PCB).

15. The method as claimed in claim 15, wherein the high-speed clock (12) is from a second PLL (36) on the ASIC which receives an input reference clock from the PCB.

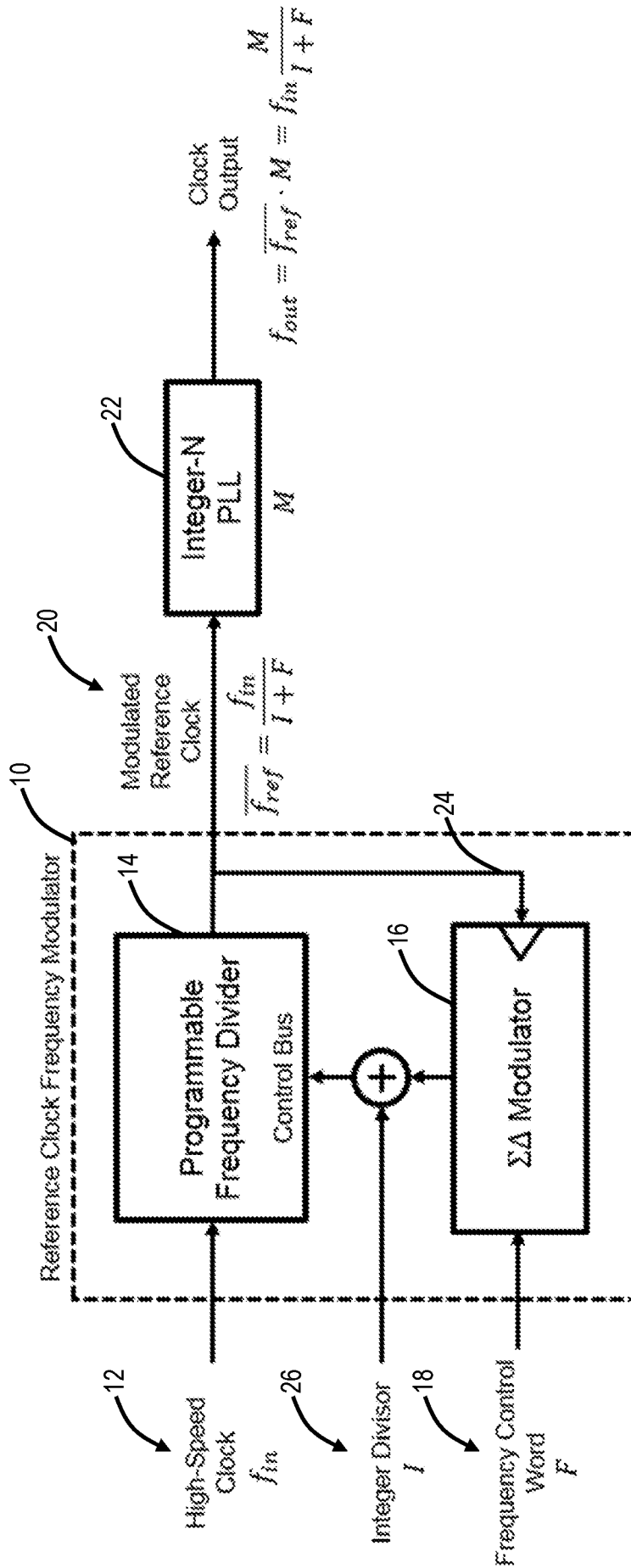


FIG. 1

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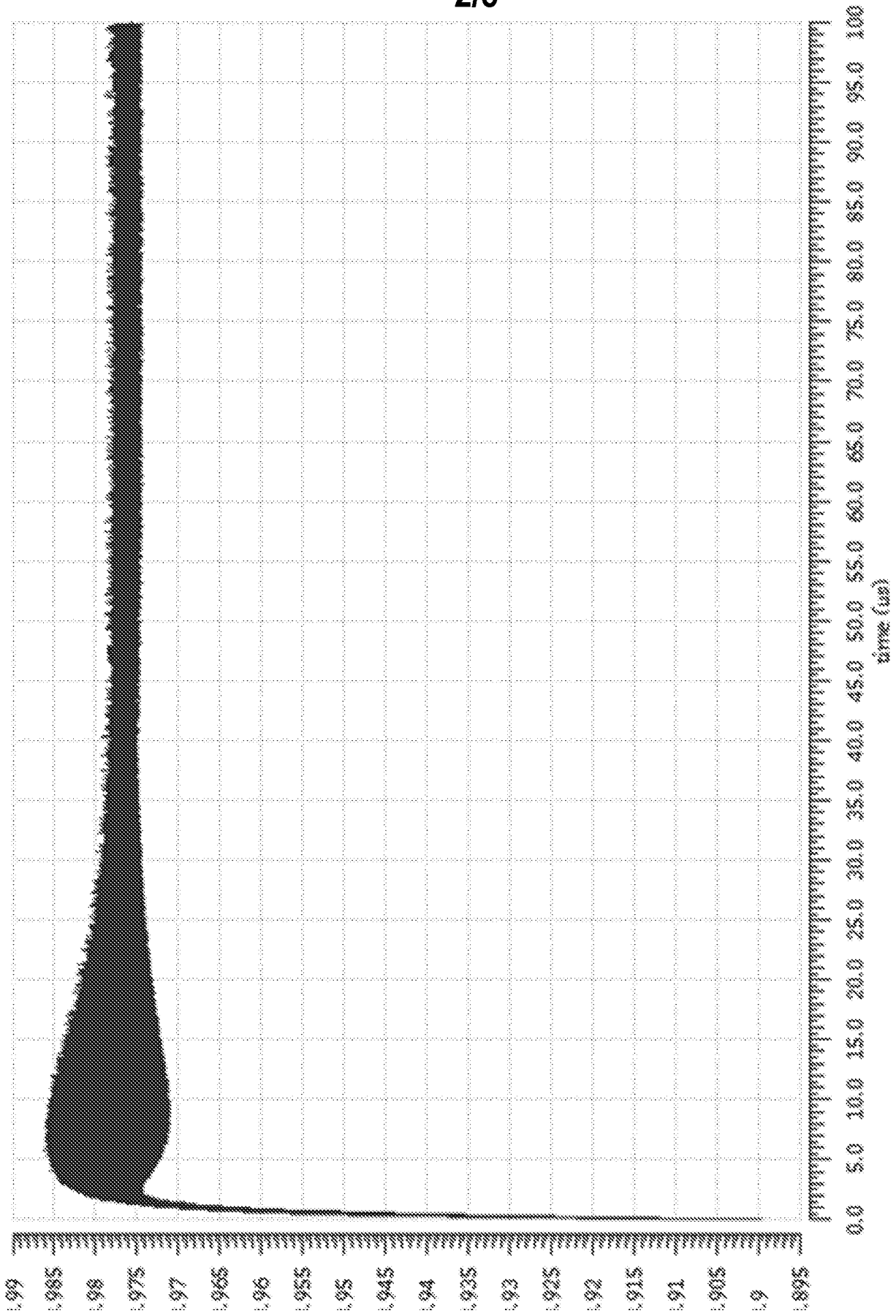


FIG. 2

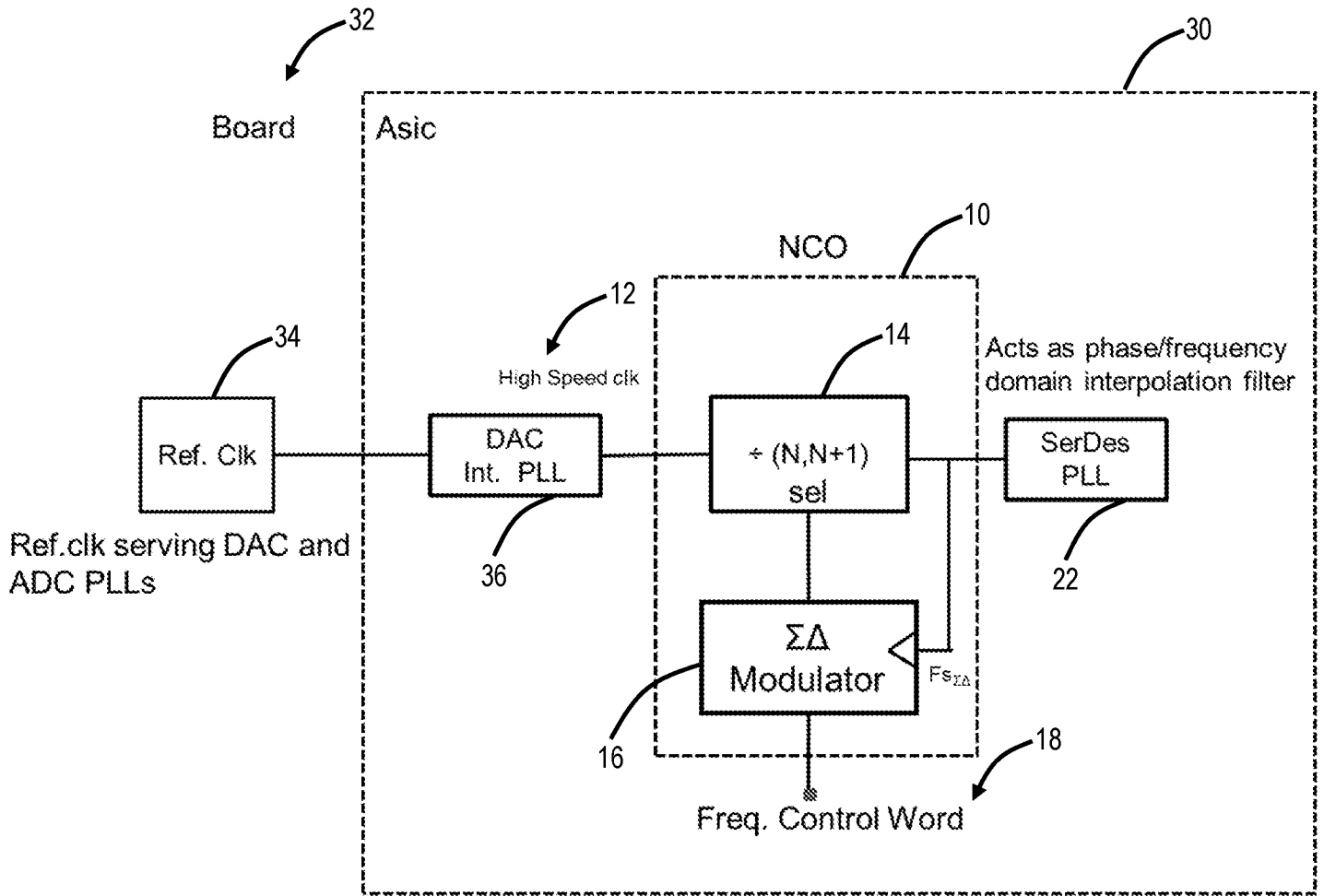


FIG. 3

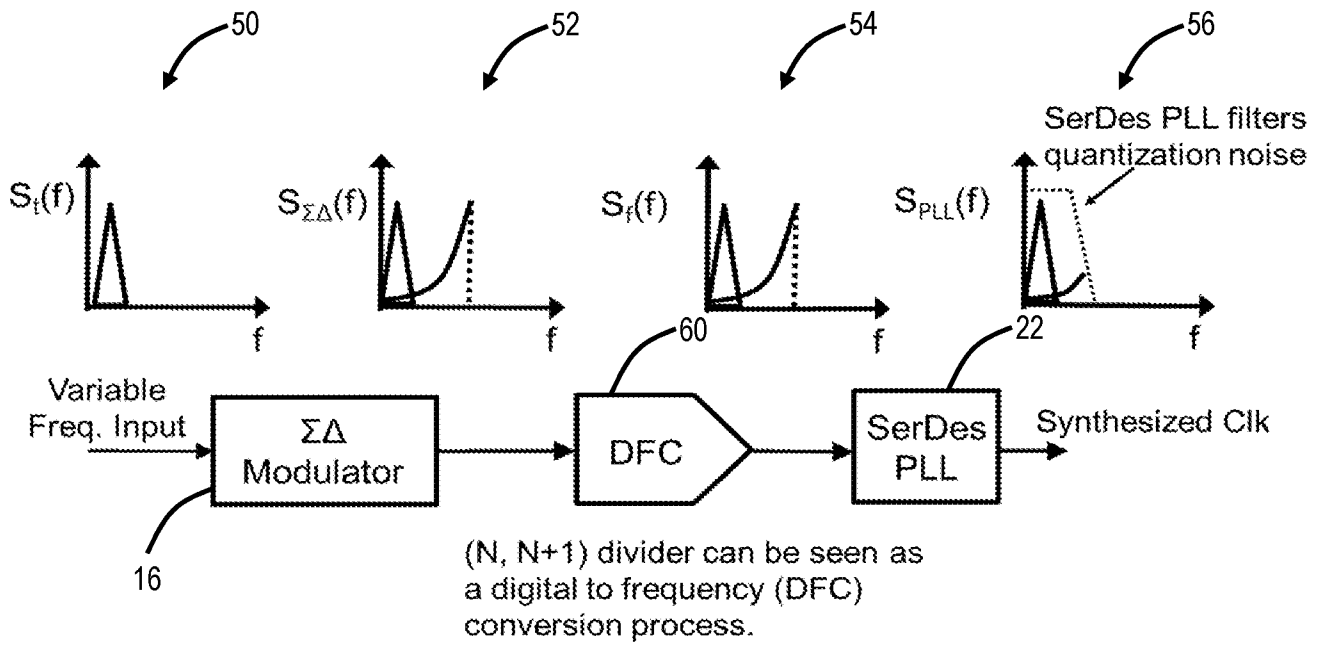
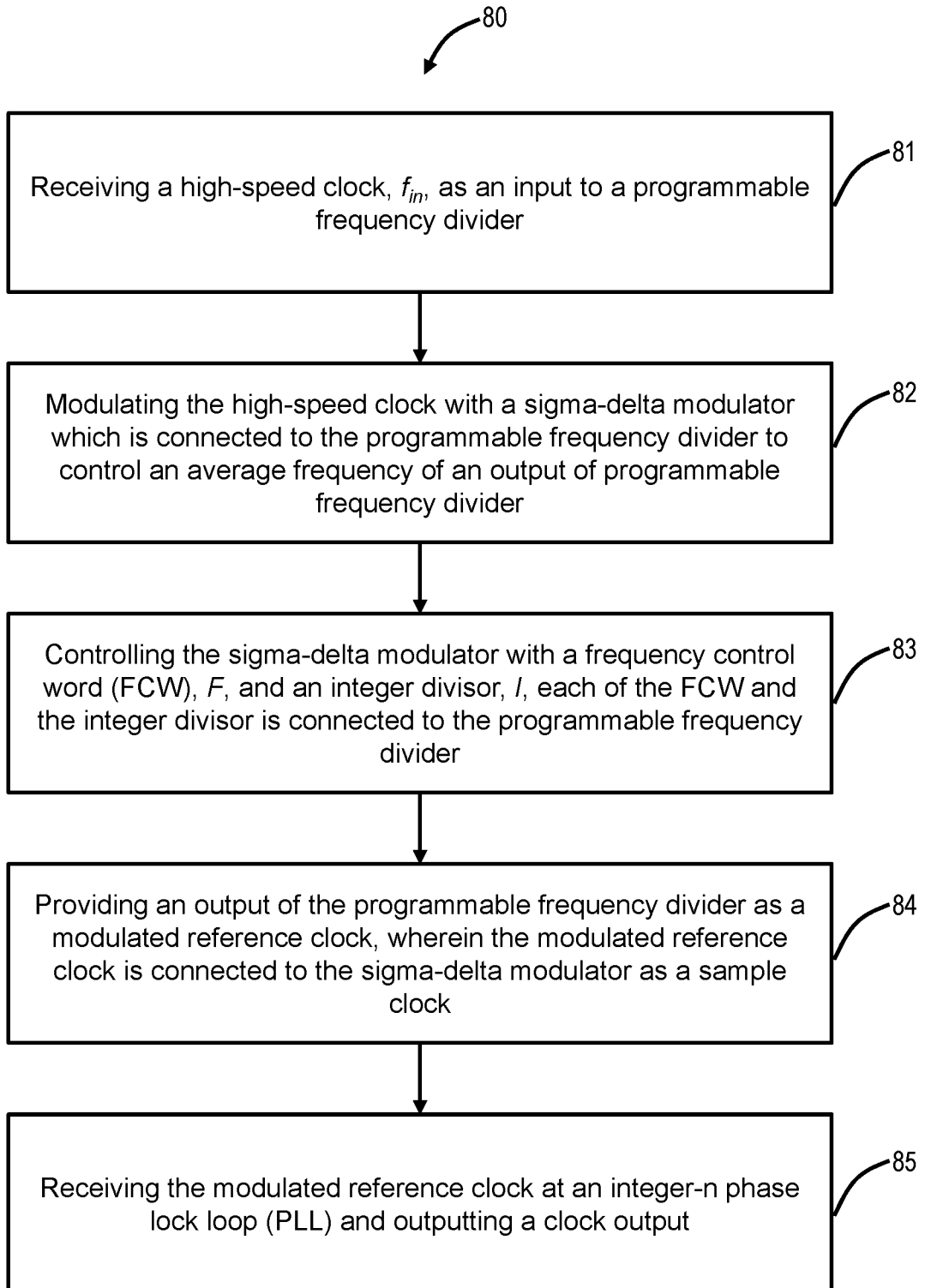


FIG. 4

5/5**FIG. 5**

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/056029

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03L7/18 H03L7/22
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/152757 A1 (SRIDHARAN KARTIK M [US]) 5 July 2007 (2007-07-05) paragraph [0045] - paragraph [0051]; figures 5-7	1-15
X	EP 1 397 772 A1 (ANALOG DEVICES INC [US]) 17 March 2004 (2004-03-17) paragraph [0076] - paragraph [0083]; figure 4	1,2, 5-10, 12-15
X	WO 2010/056813 A1 (ANALOG DEVICES INC [US]; PALMER WYN [US]; GENTILE KENNY [US]) 20 May 2010 (2010-05-20) page 2, line 19 - page 5, line 27; figures 1,2	1,2, 5-10, 12-15
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Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
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- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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- "&" document member of the same patent family

Date of the actual completion of the international search 17 December 2019	Date of mailing of the international search report 03/01/2020
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Aouichi, Mohamed
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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/056029

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>US 8 493 111 B1 (BRADLEY DONALD ANTHONY [US]) 23 July 2013 (2013-07-23)</p> <p>column 3, line 40 - column 5, line 25; figure 3</p> <p style="text-align: center;">-----</p>	<p>1,2, 7-10,14, 15</p>

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/US2019/056029

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