ISOLATED NEUROSTIMULATOR CIRCUIT

FIELD OF THE INVENTION

[0001] The present invention is generally related to electroencephalography systems, and in particular, to electrical neurostimulators for electroencephalography systems.

BACKGROUND OF THE INVENTION

[0002] Electrical neurostimulators are widely used in a variety of clinical and research contexts. These devices are commonly used for cortical stimulation in conjunction with an electroencephalography (EEG) system for functional mapping. Existing approaches to electrical stimulation have several limitations. It is desirable for a stimulator to have a high compliance voltage to allow the use of high-impedance electrodes. In some cases, voltages up to 250V may be necessary. However, circuit architectures used for neurostimulators typically expose the main current source transistor to the full compliance voltage. Since the current source is controlled by low-voltage digital and mixed-signal circuits, this approach necessitates the use of costly and esoteric analog isolation circuitry, such as photo-MOS transistors and optical isolators.

[0003] In addition to cost, analog optical isolation limits achievable stimulation bandwidth and decreases linearity and accuracy. Additional complexity arises when multiple stimulation channels are used. Existing approaches typically place all of the stimulator channels in one isolation domain, which results in poorly-controlled current paths, reducing stimulation effectiveness and increasing risk to the patient. Mitigating these added risks requires significant circuit complexity and increases cost, size, and power consumption.

SUMMARY OF THE INVENTION

[0004] One object of the present invention is to reduce complexity in neurostimulator circuits while ensuring safe operation. To better address such

concerns, in a first aspect of the invention, a neurostimulator circuit is disclosed having a galvanically isolated stimulation channel, wherein for the stimulation channel, a cascode circuit of an H-bridge circuit adjusts a voltage between a main current source and the H-bridge circuit. Such an arrangement enables all control and supervision functions to be performed by standard, low cost microcontrollers or field programmable gate arrays while minimizing additional interfaces or isolation circuitry.

[0005] In one embodiment, the neurostimulator circuit comprises an H-bridge current source circuitry comprising a first pair of switch transistors configured to operate according to a first voltage and a cascode circuit comprising a second pair of transistors; and a current source transistor configured to operate according to a second voltage and coupled to the cascode circuit; and a pair of electrodes having one of a positive or negative current driven across the pair of electrodes based on parameters received at each of the transistors of the H-bridge circuit, the current comprising a magnitude according to the current source circuit. The circuit arrangement of the H-bridge circuit and current source transistor simplifies the circuitry needed for stimulation in an electroencephalography (EEG) circuit and removes the need for costly and esoteric analog isolation circuitry.

[0006] In one embodiment, the first voltage comprises a stimulation voltage, wherein the cascode circuit is configured to transform the stimulation voltage to a second voltage (+5Vi), the second voltage lower than the stimulation voltage, the second pair of transistors configured to be operate at the stimulation voltage. The H-bridge uses high-voltage switch transistors configured as cascode source followers to reduce the maximum voltage seen by the main current source to logic levels, permitting direct connection between the high-voltage current source and the low-voltage channel controller.

[0007] In one embodiment, the neurostimulator circuit further comprises a galvanically isolated power source and galvanically isolated data interface, wherein the first stimulator channel is configured to receive isolated, low-voltage power and digital data, and optionally timing signals via the galvanically isolated power source and the galvanically isolated data interface. By placing each stimulation channel into a

dedicated isolation domain, risk to the patient is minimized, because current flow between channel circuits is not possible.

[0008] In one embodiment, the first stimulator channel is configured to provide conversion between different voltage levels according to either a DC/DC converter that is configured to convert low voltage received from the galvanically isolated power source to the first voltage suitable for stimulation or the first stimulator channel configured to receive from the galvanically isolated power source the first voltage and convert to the second voltage. For instance, for the former option, through the conversion, the DC/DC converter ensures an appropriate voltage for stimulation (e.g., 20 - 250V).

[0009] In one embodiment, wherein the cascode circuit limits a voltage at the current source transistor to below a defined isolation voltage. The cascode circuit limits the voltage on (e.g., the drain) current source transistor to below, e.g., isolation voltage of +5V, which enables high-speed, low-voltage devices to be used for the current source transistor and an error amplifier of the neurostimulator circuit, thus improving bandwidth.

[0010] In one embodiment, the neurostimulator circuit further comprises shorting the pair of electrodes to either the first voltage or ground, wherein the shorting removes charge from the pair of electrodes, wherein shorting to the first voltage precharges parasitic capacitance between the isolated first stimulator channel and a subject. That is, the neurostimulator circuit is configured with the ability to short the electrodes to either the high voltage (e.g., +HV) or ground (e.g., the isolated ground rails). Charge balance should be maintained during stimulation to prevent polarization and unwanted chemical reactions at a skin-electrode interface. Since it is not possible to guarantee perfect matching between the total charge of the positive and negative halves of the stimulation waveform, a small amount of imbalance charge may build up on the electrode capacitance after every stimulation pulse train. Shorting the electrodes between stimulation pulses is a simple and effective way of removing this charge. Shorting the electrodes to the +HV rail is also an effective way of precharging the parasitic capacitance between the isolated channel and the patient, thus avoiding

artifacts and excessive current flow at the beginning of the stimulation pulse, or when switching polarity.

[0011] In one embodiment, the current source unit further comprises an isolation-side channel controller configured to provide parameters to the H-bridge circuit, the transistors of the H-bridge circuit controlled by the channel controller to close at most one of the transistors on each side of the H-bridge circuit at one time, wherein the channel controller controls operations of the first stimulator channel, the operations including generating the voltage corresponding to current input to the error amplifier and providing the parameters. Placing the channel controller on the isolated side eliminates the need to send analog signals across a galvanic isolation barrier.

[0012] In one embodiment, the channel controller of the neurostimulator circuit is further configured to monitor one or more points of the current source unit and to enforce subject safety measures based on the monitoring, wherein enforcement includes configuring the first stimulator channel to a failsafe state. Measured parameters may include compliance voltage (e.g., the drain of the current source transistor), return current sense voltage, and supply current sense voltage. Faults in the current source circuit may result in a mismatch between the supply and return currents and/or a mismatch between the programmed and sensed currents. Thus, the neurostimulator circuit comprises functionality to ensure patient safety.

[0013] In one embodiment, the neurostimulator circuit comprises the channel controller and a system controller that are configured to provide parallel supervision. In effect, the two controllers operate to collectively bolster fail-safe operation.

[0014] These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Many aspects of the invention can be better understood with reference to the following drawings, which are diagrammatic. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the

principles of the present invention. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

[0016] FIG. 1 is a schematic diagram that illustrates an example system in which a neurostimulator circuit may be used, in accordance with an embodiment of the invention.

[0017] FIG. 2 is a schematic diagram that further illustrates an example neurostimulator circuit, in accordance with an embodiment of the invention.

[0018] FIG. 3 is a schematic diagram that further illustrates select components of the neurostimulator circuit of FIG. 2, in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[0019] Disclosed herein are certain embodiments of a neurostimulator circuit that comprises a system controller and one or more mutually galvanically isolated stimulation channels, each having a channel controller and stimulation circuitry that includes a cascode architecture and a current source device. The cascode architecture enables a conversion of operational voltages between an H-bridge circuit and a current source device/circuit, and in one embodiment, a cascode circuit reduces the operating voltage of the current source device and enables direct connection to the channel controller. This arrangement enables individual channels to be galvanically isolated from each other, improving safety and performance while minimizing component count.

[0020] Digressing briefly, typical neurostimulators expose the main current source transistor to the full compliance voltage, necessitating the use of costly and esoteric analog isolation circuitry. Additionally, some neurostimulators typically place all of the stimulator channels in one isolation domain, which results in poorly-controlled current paths, reducing stimulation effectiveness and increasing risk to the patient. In certain embodiments of a neurostimulator circuit, cascode transistors capable of withstanding a stimulation voltage are used to reduce the voltage seen by the main

current source transistor, permitting direct connection between the high-voltage (stimulation voltage) current source and the low-voltage channel controller. Further, certain embodiments of a neurostimulator circuit places each stimulation channel into a dedicated isolation domain, and places the channel controller on the isolated side to eliminate the need to send analog signals across the galvanic isolation barrier. Risk to the patient is minimized, because current flow between channel circuits is not possible.

[0021] Having summarized certain features of a neurostimulator circuit of the present disclosure, reference will now be made in detail to the description of a neurostimulator circuit as illustrated in the drawings. While a neurostimulator circuit will be described in connection with these drawings, there is no intent to limit it to the embodiment or embodiments disclosed herein. Further, although the description identifies or describes specifics of one or more embodiments, such specifics are not necessarily part of every embodiment, nor are all of any various stated advantages necessarily associated with a single embodiment. On the contrary, the intent is to cover all alternatives, modifications and equivalents included within the principles and scope of the disclosure as defined by the appended claims. For instance, two or more embodiments may be interchanged or combined in any combination. Further, it should be appreciated in the context of the present disclosure that the claims are not necessarily limited to the particular embodiments set out in the description.

[0022] Note that reference herein to a high voltage (HV) refers to a voltage suitable for providing a suitable stimulation current across a pair of electrodes in a neurostimulator system, for instance, in an electroencephalography (EEG) system, though not limited to that environment.

[0023] Referring to FIG. 1, shown is an example system in which a neurostimulator circuit may be used. In general, the neurostimulator circuit described herein may be used for functional mapping for both research and clinical use (e.g., during neurosurgery). The neurostimulator circuit may also be used in implanted and non-invasive neurostimulator devices for treatment of epilepsy, depression, pain management, motor rehabilitation, and others. For instance, current research involves developing transcranial direct current stimulation (tDCS) for a variety of potential uses,

including cognitive training, memory enhancement, etc. The neurostimulator circuit described herein is particularly suitable for non-invasive tDCS devices. Shown in the example illustrated in FIG. 1 is an example EEG system 10 that includes a neurostimulator circuit 12 that delivers stimulation signals to a plurality of electrodes that that are collectively arranged as a net 14, the net 14 fitted on the head of a subject 16 (e.g., the electrodes positioned on the scalp of the subject 16). Note that, although the example environment depicted in FIG. 1 comprises an electroencephalography system, this environment represents one environment among others that may use and benefit from a neurostimulator circuit 12. The net 14 may include 32, 64,128, or 256 EEG sensors/electrodes. The number of stimulator channels may be a subset of the amount of electrodes (e.g., twenty-six (26) stimulator channels) that are selected via a switch matrix (FIG. 2). The neurostimulator circuit 12 further comprises a system controller 18 that provides data to a plurality of stimulator channels 20. In one embodiment, the system controller 18 is configured to generate a plurality of stimulation parameters associated with a plurality of respective stimulator channels 20. The plurality of stimulator channels 20 are mutually, galvanically isolated, wherein each stimulator channel includes a channel controller 22. In other words, each channel 20 is isolated from every other channel 20, each channel 20 serving as a floating current source. The system controller 18 communicates the stimulation parameters to the respective channel controllers 22.

[0024] FIG. 2 further illustrates an example neurostimulator circuit for one channel (Channel 1) of the plural channels 20, denoted as channel 20A of the EEG system 10 of FIG. 1, with emphasis on the neurostimulator circuit 12 for a subset of electrodes of the net 14. As noted above, the neurostimulator circuit 12 may be used in other systems that provide a stimulation current across electrodes, and hence is not limited to the EEG system 10. As noted by the dashes, the neurostimulator circuit for channel 1 20A, and operations performed in cooperation with the system controller 18, is essentially duplicated for the other channels (e.g., Channels 2 through N), and hence the description below for channel 1 20A is applicable to the other channels. Emphasis is placed on the neurostimulator circuit for channel 1 20A and its cooperation with the

system controller 18, with the understanding that operations of the neurostimulator circuit for other channels and their respective cooperation with the system controller 18 similarly applies. It should be appreciated by one having ordinary skill in the art, in the context of the present disclosure, that variations to the example arrangement depicted in FIG. 2 may be implemented to serve a similar function, and hence are contemplated to be within the scope of the present disclosure.

[0025] As shown, the neurostimulator circuit 12 comprises the system controller 18. The system controller 18 generates the appropriate stimulation parameters, communicates them (TX) to the channel controller 22A (e.g., and the other controllers similarly), and monitors system operation (RX) and safety (for example, by monitoring current consumed by stimulation channel 20A (and others) and periodically polling the status of the channel controller 22A (and others)). The stimulation parameters and sites may be chosen by a researcher or medical practitioner. In some embodiments, a treatment planning tool (e.g., software) that helps the user select the optimal electrodes and current levels to target a particular region of the brain may be used or the user may specify the parameters manually.

[0026] The system controller 18 communicates with the channel controller 22A. Galvanic isolation for both power and data is between the individual stimulator channels and the main system controller 18 (e.g., via galvanically isolated power and data). In one embodiment, the channel 1 20A receives digital data via a galvanically isolated, digital data interface 24 and power via a galvanically isolated power source 26. The galvanically isolated digital interface 24 may comprise an asynchronous serial port, synchronous SPI (serial peripheral interface) port, I2C, CAN (controlled area network), Ethernet, digital optocoupler, etc. This digital interface 24 transmits digital data (DIGI DTA) and optionally timing signals (TIMING). In general, galvanic isolation may be optical, inductive, capacitive, or radio frequency based.

[0027] The neurostimulator circuit of the channel 1 20A comprises the channel controller 22A and the isolated power source 26. In general, the channel 1 20A receives galvanically isolated low-voltage power thorough the isolated power source 26. In one embodiment, the isolated power source 26 may be a transformer-isolated

DC/DC converter, such as an off-the-shelf module. Other types of isolated DC/DC converters may be used as the isolated power source 26, including capacitively or optically coupled devices.

[0028] The channel controller 22A may be embodied as one or more processing elements or components. In one embodiment, the channel controller 22A comprises a field programmable gate array (FPGA) device (and any associated interface circuitry). In some embodiments, the channel controller 22A comprises a microcontroller (MCU) with one or more processing cores. The channel controller 22A controls the operation of the stimulator channel 1 20A. In one embodiment, and as explained further below, one function of the controller 22A is to generate a voltage proportional to the programmed current on an ISET output (described below). Another function of the controller 22A is to control the operation of plural switches of an H-Bridge circuit to generate the appropriate waveform on the patient electrodes. In effect, through the arrangement of each neurostimulator circuit of the neurostimulator circuit 12 depicted in FIG. 2 and described herein, the controller 22A may be implemented as a standard, low-cost microcontroller or FPGA, with a minimum of additional interfaces or isolation circuitry, to provide for control and supervision functions of the channel 1 20A.

[0029] Explaining further, the controller 22A receives parameters from the system controller 18, including the programmed current magnitude, polarity, pulse width or other waveform parameters, including any safety limits on current or compliance voltage. Such functionality may be achieved in any one of a plurality of ways. For instance, the controller 22A may be configured as a dumb client, where it receives the waveform point-by-point from the system controller 18 and merely performs control and safety functions for the analog train. In another example implementation, the controller 22A has more intelligence, where it is configured to synthesize more complex waveforms without intervention from the system controller 18. In this latter case, periodic synchronization signals may still be received to ensure all the channel controllers 22 are running in lockstep. The controller 22A is configured to provide a periodic report back to the system controller 18. The report back may be as rudimentary as a keep alive signal to ensure the controller 22A is operational, or the

report back may include other or additional information including actual output current, compliance voltage, and any error flags.

[0030] The neurostimulator circuit of the channel 1 20A further comprises a DC/DC converter (DC/DC) 28, H-bridge/current source circuitry (HBRDG) 30, and safety monitor circuit (MNTR) 32 all coupled to the controller 22A. Attention is directed to FIG. 3 with continued reference to FIG. 2 for these and other elements of the neurostimulator circuit of the channel 1 20A. Shown in FIG. 3 is the isolated power source 26, which in this example shows a low voltage +5V (volts) and isolated low voltage +5Vi. Also shown with the inverted triangle symbol is ground and isolated (ISO) ground. The controller 22A, which receives as input (from the system controller 18) the digital data and optional timing signals via the isolated data interface 24, is shown as a chip with additional inputs ISENSE1 and ISENSE2 corresponding to signals monitored from the H-bridge/current source circuitry 30, and the following outputs provided to the H-bridge/current source circuitry 30: ISET (current source setting), SW_HN (switch high, negative polarity), SW_LN (switch low, negative polarity), SW-HP (switch high, positive polarity), SW_LP (switch low, positive polarity). The controller 22A also includes output HV_EN for provision to the DC/DC converter 28 (e.g., high-voltage enable).

[0031] The DC/DC converter 28 receives low voltage, isolated power (LV PWR, e.g., +5Vi) from the isolated power source 26, and is configured to receive a high voltage enable signal (HV-EN) from the controller 22A. That is, HV-EN is a high voltage enable signal that enables the DC/DC converter 28, with functionality including shut-down to save power when the current source is not being used and/or when a fault is detected, to place the channel into a safe state. In one embodiment, the DC/DC converter 28 comprises a step-up converter that converts the low voltage power (e.g., +5Vi) to the appropriate high voltage (HV) power for stimulation (typically in the range of 20 - 250V). Note that in some embodiments, the isolated power source 26 may provide high-voltage power to the channel 20A, wherein the channel generates, for instance, +5Vi. In one embodiment, the DC/DC converter 28 may employ a variable conversion ratio (CR) to minimize power consumption with different electrode

impedances and stimulation current ranges. In other words, the conversion ratio allows the voltage to be reduced to improve efficiency when electrode impedance is low (e.g., as selected by a user and/or automatically adjusted based on electrode impedance). For instance, the DC/DC converter 28 may comprise a non-isolated boost converter, in which case the conversion ratio is controlled by a duty cycle of the boost converter switch(es) (e.g., the main switching element of the boost converter, such as using a switch and diode or multiple switches). The logic for performing that function may be provided by the controller 22A. In some embodiments, the ratio may be adjusted dynamically to maintain current source compliance by measuring the voltage at the drain of M5 (of current source circuit 34) during stimulation and adjusting the conversion ratio to maintain a sufficient compliance margin. For instance, the conversion ratio may be selected by first measuring an electrode impedance by reducing the output of the DC/DC converter 28 until the voltage on the drain of the current source circuit 34 (drain of M5) drops below its normal value during a pulse (e.g., which is approximately equal to the voltage on the +5Vi supply rail minus the threshold voltage of M3). The output voltage may then be increased slightly. In some embodiments, this procedure may be performed periodically during stimulation.

[0032] The H-bridge/current source circuitry 30, also referred to herein as a current source unit, comprises the current source circuit 34 and an H-bridge circuit 36. In one embodiment, the H-bridge circuit 36 comprises switch (e.g., field-effect transistors (FETs M1, M2)) and cascode transistors (FETs, M3, M4). Coupled to the gate of the switch gates M1, M2 are high voltage (HV) inverter amplifiers (LS) that receive the parameters (SW_HN, SW_HP) from the controller 22A, and coupled to the cascode FETs M3, M4 are low voltage (e.g., +5Vi) non-inverter amplifiers that receive parameters (SW_LN, SW_LP) from the controller 22A. The current source circuit 34 comprises a current source FET (M5), a sense resistor (R1), and an error amplifier (A2) that receives ISET from the controller 22A. ISET is the programmed stimulation current magnitude. Though ISET represents an output of the controller 22A, it is ultimately based on the values configured by a user as explained above. Note that FETs are used for illustration, and that in some embodiments, other types of switching devices

may be used. Note that the arrangement depicted in FIG. 3 is one illustrative embodiment, and that in some embodiments may have a different arrangement. For instance, in some embodiments, the circuit may be configured in a manner that is inverted or upside-down from what is depicted in FIG. 3, where the current source is connected to the HV rails and the H-bridge circuit is on the low side. Also, though shown with inverter and non-inverter configurations, other circuits may be used to perform the same functionality (e.g., where the H-bridge circuit switches are controlled such that at most one switch on each side of the H-bridge circuit is closed at a time).

[0033] To generate both positive and negative currents, the switches (M1, M2) and cascode (M3, M4) FETs are configured as an H-bridge configuration. For example, to produce a current from a positive (+) electrode to a negative (–) electrode of electrode pair 38, SW_HP and SW_LN are driven high, while SW_LP and SW_HN are driven low, which turns on M2 and M3 and turns off M1 and M4. ISET is driven with a voltage proportional to the desired current, where the error amplifier A2 adjusts the current through M5 so that it is equal to V/R (e.g., V(ISET)/R1). The cascode devices M3/M4 limit the voltage on the drain of M5 to below the isolated low voltage value (e.g., V(+5Vi)), enabling high-speed, low-voltage devices to be used for M5 and A2, thus improving bandwidth.

[0034] As noted above, the H-bridge 36 uses high-voltage switch transistors (M1, M2) configured as cascode source followers to reduce the maximum voltage seen by the main current source (M5) to logic levels. It may be desirable to use a high voltage, such as +250V, for the HV power rail in order to accommodate high-impedance electrodes. If the electrode impedance is low and if cascoding were not used, the current source M5 would have to withstand the full stimulation voltage, and the transistor M5 should then be a high-voltage device, and thus have higher parasitic capacitances for the same current rating, limiting performance (response time and bandwidth) due to the Miller effect. In addition, the amplifier A2 may potentially require additional circuitry to suppress high-voltage spikes through the Cgd parasitic capacitance when the current source turns on and off. According to certain embodiments of neurostimulator circuit, transistors M1-M4 are the only devices that

“see” the full 250V, and since they are acting simply as switches, their parasitics do not significantly affect performance. The Miller effect is neutralized by cascoding (the drain of M5 is at a substantially constant voltage when the current source is active). Furthermore, it is easy to connect the drain of M5 directly to an ADC input of the controller 22A to monitor compliance voltage, without requiring additional high-voltage capable amplifiers or voltage dividers.

[0035] Other features of this neurostimulator circuit configuration includes the ability to short the electrodes to either the +HV or the ISOGND rails. For instance, it is important to maintain charge balance during stimulation to prevent polarization and unwanted chemical reactions at the skin-electrode interface. Since it is not possible to guarantee perfect matching between the total charge of the positive and negative halves of the stimulation waveform, a small amount of imbalance charge may build up on the electrode capacitance after every stimulation pulse train. Shorting the electrodes between stimulation pulses is a simple and effective way of removing this charge. Shorting the electrodes to the +HV rail is also an effective way of precharging the parasitic capacitance between the isolated channel and the patient, thus avoiding artifacts and excessive current flow at the beginning of the stimulation pulse, or when switching polarity.

[0036] Note that the H-bridge/current source circuitry 30 is shown in FIG. 2 as stimulating the electrodes 38 via a switch matrix 40. In general, each stimulator channel 20 has its own isolated power source 26, resulting in each stimulator channel 20 comprising a floating 2-terminal current source. Notably, there is not a 1:1 relationship between stimulator channels 20 and electrodes 38. For example, the neurostimulator circuit 12 may have thirty-two (32) stimulator channels 20 (with two output terminals each), and in a HD EEG system, the output terminals are connected to a programmable subset of the 256 electrodes using the switch matrix 40.

[0037] The channel controller 22A is also responsible for monitoring system status to ensure patient safety. In one embodiment, the measured parameters may include compliance voltage (drain of M5), return current sense voltage V(ISENSE1), and/or the supply current sense voltage V(ISENSE2 measured by safety monitor circuit

32). Faults in the current source circuit will result in a mismatch between the supply and return currents and/or a mismatch between the programmed and sensed currents. Upon detection of a fault, the controller 22A can put the circuit in a failsafe state by disabling the DC/DC converter 28 and turning off all switches. In some embodiments, the system controller 18 may shut down the isolated power source 26 to the faulty channel and/or disconnect the patient electrodes 38 from the current source outputs.

[0038] To ensure safety against single faults, the controller 22A may incorporate auxiliary safety monitoring circuits (AUX SPV) 42, which may include watchdog timers and auxiliary processing elements. For example, the controller 22A may comprise an FPGA, and the auxiliary safety monitoring circuits 42 may provide parallel supervision. If either processing unit 22A or 42 detects a fault or is unable to communicate with the other unit, it may generate a fault signal and the channel put in a failsafe state. In some embodiments, this parallel supervision may be performed between the controller 22A and the system controller 18, or any combination of the controller 22A, system controller 18, and auxiliary safety monitoring circuits 42.

[0039] Note that the system controller 18 and channel controller 22 may be implemented with any or a combination of the following technologies, which are all well-known in the art: a discrete logic circuit(s) having logic gates for implementing logic functions upon data signals, an application specific integrated circuit (ASIC) having appropriate combinational logic gates, a programmable gate array(s) (PGA), a field programmable gate array (FPGA), TPUs, GPUs, and/or other accelerators/co-processors, etc.

[0040] In one embodiment, a neurostimulator circuit is disclosed, comprising: a galvanically isolated first stimulator channel, comprising a current source unit, the current source unit comprising: an H-bridge circuit comprising a first pair of switch transistors configured to operate according to a first voltage and a cascode circuit comprising a second pair transistors; and a current source circuit configured to operate according to a second voltage and coupled to the cascode circuit; and a pair of electrodes having one of a positive or negative current driven across the pair of

electrodes based on parameters received at each of the transistors of the H-bridge circuit, the current comprising a magnitude according to the current source circuit.

[0041] In one embodiment, the preceding neurostimulator circuit, wherein the first voltage comprises a stimulation voltage, wherein the cascode circuit is configured to transform the stimulation voltage to a second voltage, the second voltage lower than the stimulation voltage, the second pair of transistors configured to be operate at the stimulation voltage.

[0042] In one embodiment, any one of the preceding neurostimulator circuits, further comprising a galvanically isolated power source and a galvanically isolated data interface, wherein the first stimulator channel is configured to receive isolated, low-voltage power and digital data, and optionally timing signals via the galvanically isolated power source and the galvanically isolated data interface.

[0043] In one embodiment, any one of the preceding neurostimulator circuits, wherein the first stimulator channel is configured to provide conversion between different voltage levels according to either a DC/DC converter that is configured to convert low voltage received from the galvanically isolated power source to the first voltage suitable for stimulation or the first stimulator channel configured to receive from the galvanically isolated power source the first voltage and convert to the second voltage.

[0044] In one embodiment, any one of the preceding neurostimulator circuits, wherein the DC/DC converter is configured to convert the low voltage power based on either a variable conversion ratio and a plurality of stimulation values or a conversion ratio that is dynamically adjusted based on a comparison of a measured value corresponding to a transistor of the current source circuit and a predetermined current source compliance value.

[0045] In one embodiment, any one of the preceding neurostimulator circuits, wherein the current source unit further comprises an error amplifier and a sense resistor, wherein the error amplifier adjusts a current through the transistor of the current source circuit according to a voltage at the error amplifier relative to a resistance at the sense resistor.

[0046] In one embodiment, any one of the preceding neurostimulator circuits, wherein the cascode circuit limits a voltage at the transistor of the current source circuit to below a defined isolation voltage.

[0047] In one embodiment, any one of the preceding neurostimulator circuits, further comprising shorting the pair of electrodes to either the first voltage or ground, wherein the shorting removes charge from the pair of electrodes or wherein shorting to the first voltage precharges parasitic capacitance between the isolated first stimulator channel and a subject.

[0048] In one embodiment, any one of the preceding neurostimulator circuits, wherein the current source unit further comprises an isolation-side channel controller configured to provide parameters to the H-bridge circuit, the transistors of the H-bridge circuit controlled by the channel controller to close at most one of the transistors on each side of the H-bridge circuit at one time, wherein the channel controller controls operations of the first stimulator channel, the operations including generating the voltage corresponding to current input to the error amplifier and providing the parameters.

[0049] In one embodiment, any one of the preceding neurostimulator circuits, wherein the channel controller is further configured to monitor one or more points of the current source unit and to enforce subject safety measures based on the monitoring, wherein enforcement includes configuring the first stimulator channel to a failsafe state.

[0050] In one embodiment, any one of the preceding neurostimulator circuits, wherein the failsafe state comprises one or more of disabling the DC/DC converter or turning off all transistors of the H-bridge circuit.

[0051] In one embodiment, any one of the preceding neurostimulator circuits, further comprising a system controller coupled to the channel controller via the galvanically isolated digital interface and the galvanically isolated power source.

[0052] In one embodiment, any one of the preceding neurostimulator circuits, wherein the system controller is configured to enforce subject safety measures by one or more of shutting down power to the first stimulator channel via the galvanically isolated power source or disconnecting the pair of electrodes.

[0053] In one embodiment, any one of the preceding neurostimulator circuits, wherein the channel controller and system controller or auxiliary safety monitoring circuit are configured to provide parallel supervision.

[0054] In one embodiment, any one of the preceding neurostimulator circuits, further comprising one or more additional stimulator channels each configured according to the first stimulator channel and in communication with the system controller.

[0055] While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims. Note that various combinations of the disclosed embodiments may be used, and hence reference to an embodiment or one embodiment is not meant to exclude features from that embodiment from use with features from other embodiments. In the claims, the word “comprising” does not exclude other elements or steps, and the indefinite article “a” or “an” does not exclude a plurality. A single processor or other unit may fulfill the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. A computer program may be stored/distributed on a suitable medium, such as an optical medium or solid-state medium supplied together with or as part of other hardware, but may also be distributed in other forms. Any reference signs in the claims should be not construed as limiting the scope.

CLAIMS

At least the following is claimed:

1. A neurostimulator circuit (12), comprising:

a galvanically isolated first stimulator channel, comprising a current source unit (30), the current source unit comprising:

an H-bridge circuit (36) comprising a first pair of switch transistors (M1, M2) configured to operate according to a first voltage and a cascode circuit comprising a second pair transistors (M3, M4); and

a current source circuit (34) configured to operate according to a second voltage and coupled to the cascode circuit; and

a pair of electrodes (38) having one of a positive or negative current driven across the pair of electrodes based on parameters received at each of the transistors of the H-bridge circuit, the current comprising a magnitude according to the current source circuit.

2. The neurostimulator circuit of the preceding claim, wherein the first voltage comprises a stimulation voltage, wherein the cascode circuit is configured to transform the stimulation voltage to a second voltage (+5Vi), the second voltage lower than the stimulation voltage, the second pair of transistors configured to be operate at the stimulation voltage.

3. The neurostimulator circuit of any one of the preceding claims, further comprising a galvanically isolated power source (26) and a galvanically isolated data interface, wherein the first stimulator channel is configured to receive isolated, low-voltage power and digital data, and optionally timing signals via the galvanically isolated power source and the galvanically isolated data interface.

4. The neurostimulator circuit of any one of the preceding claims, wherein the first stimulator channel is configured to provide conversion between different voltage levels according to either a DC/DC converter (28) that is configured to convert low voltage (+5Vi) received from the galvanically isolated power source to the first voltage suitable for stimulation or the first stimulator channel configured to receive from the galvanically isolated power source the first voltage and convert to the second voltage.

5. The neurostimulator circuit of any one of the preceding claims, wherein the DC/DC converter is configured to convert the low voltage power based on either a variable conversion ratio and a plurality of stimulation values or a conversion ratio that is dynamically adjusted based on a comparison of a measured value corresponding to a transistor (M5) of the current source circuit and a predetermined current source compliance value.

6. The neurostimulator circuit of any one of the preceding claims, wherein the current source unit further comprises an error amplifier (A2) and a sense resistor (R1), wherein the error amplifier adjusts a current through the transistor of the current source circuit according to a voltage at the error amplifier relative to a resistance at the sense resistor.

7. The neurostimulator circuit of any one of the preceding claims, wherein the cascode circuit limits a voltage at the transistor of the current source circuit to below a defined isolation voltage.

8. The neurostimulator circuit of any one of the preceding claims, further comprising shorting the pair of electrodes to either the first voltage or ground, wherein the shorting removes charge from the pair of electrodes or wherein shorting to the first voltage precharges parasitic capacitance between the isolated first stimulator channel and a subject.

9. The neurostimulator circuit of any one of the preceding claims, wherein the current source unit further comprises an isolation-side channel controller (22A) configured to provide parameters to the H-bridge circuit, the transistors of the H-bridge circuit controlled by the channel controller to close at most one of the transistors on each side of the H-bridge circuit at one time, wherein the channel controller controls operations of the first stimulator channel, the operations including generating the voltage corresponding to current input to the error amplifier and providing the parameters.

10. The neurostimulator circuit of any one of the preceding claims, wherein the channel controller is further configured to monitor one or more points of the current source unit and to enforce subject safety measures based on the monitoring, wherein enforcement includes configuring the first stimulator channel to a failsafe state.

11. The neurostimulator circuit of any one of the preceding claims, wherein the failsafe state comprises one or more of disabling the DC/DC converter or turning off all transistors of the H-bridge circuit.

12. The neurostimulator circuit of any one of the preceding claims, further comprising a system controller (18) coupled to the channel controller via the galvanically isolated digital interface and the galvanically isolated power source.

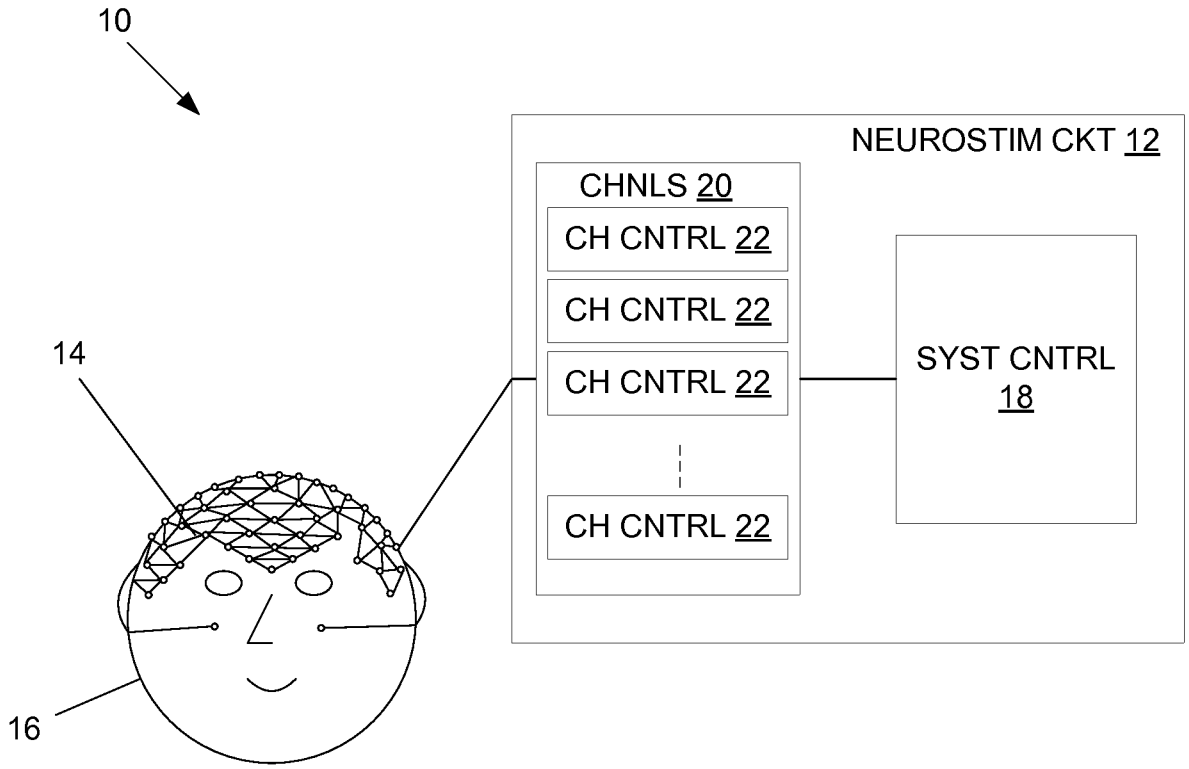
13. The neurostimulator circuit of any one of the preceding claims, wherein the system controller is configured to enforce subject safety measures by one or more of shutting down power to the first stimulator channel via the galvanically isolated power source or disconnecting the pair of electrodes.

14. The neurostimulator circuit of any one of the preceding claims, wherein the channel controller and system controller or auxiliary safety monitoring circuit (42) are configured to provide parallel supervision.

15. The neurostimulator circuit of any one of the preceding claims, further comprising one or more additional stimulator channels each configured according to the first stimulator channel and in communication with the system controller.

ABSTRACT OF THE DISCLOSURE

A neurostimulator circuit (12) having a galvanically isolated stimulation channel (20), wherein for the stimulation channel, a cascode circuit of an H-bridge circuit adjusts a voltage between a main current source and the H-bridge circuit.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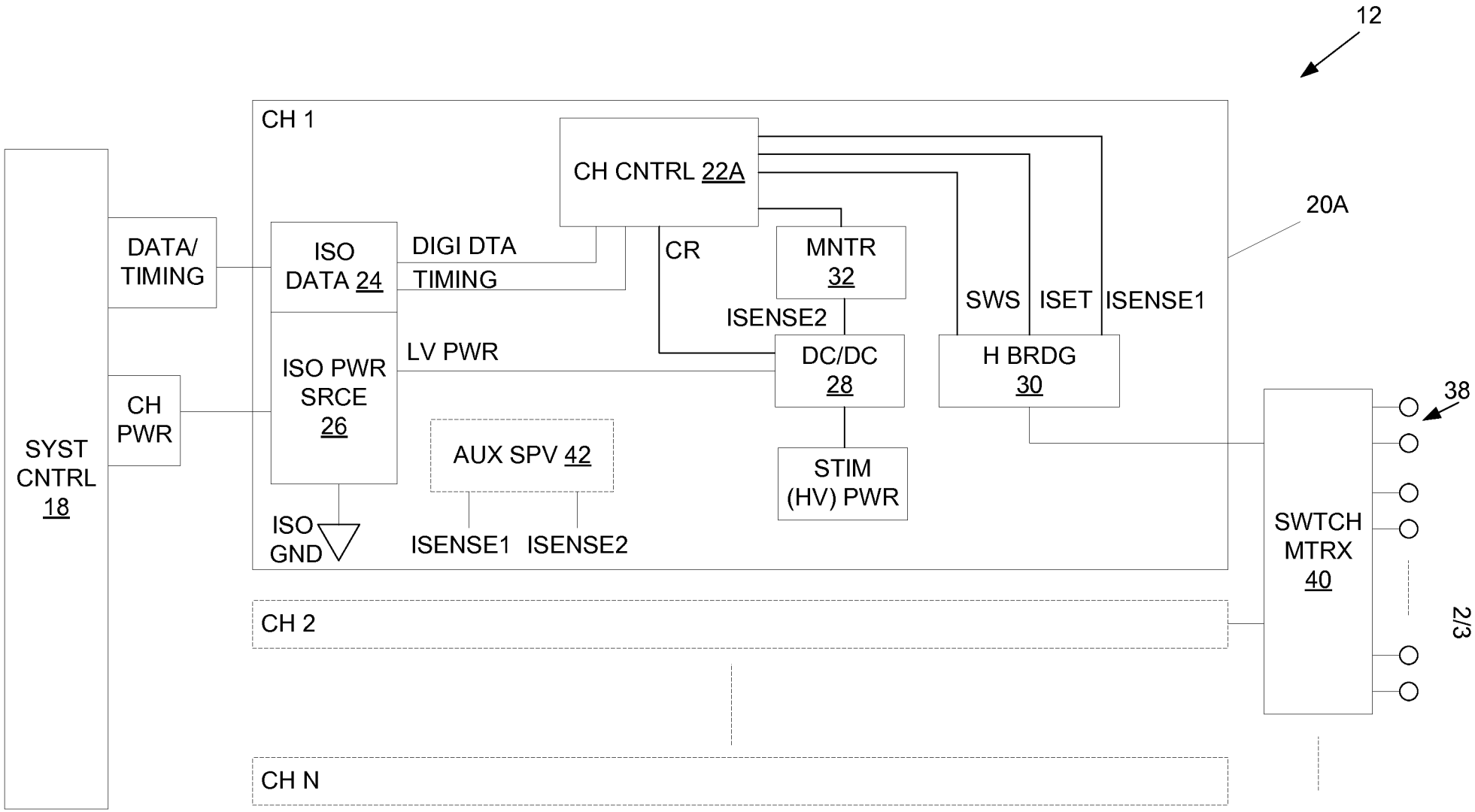
14
16

FIG. 1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LV PWR
DC/DC
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H BRDG
30
38
SYST
CNTRL
18
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ISO PWR
SRCE
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FIG. 2

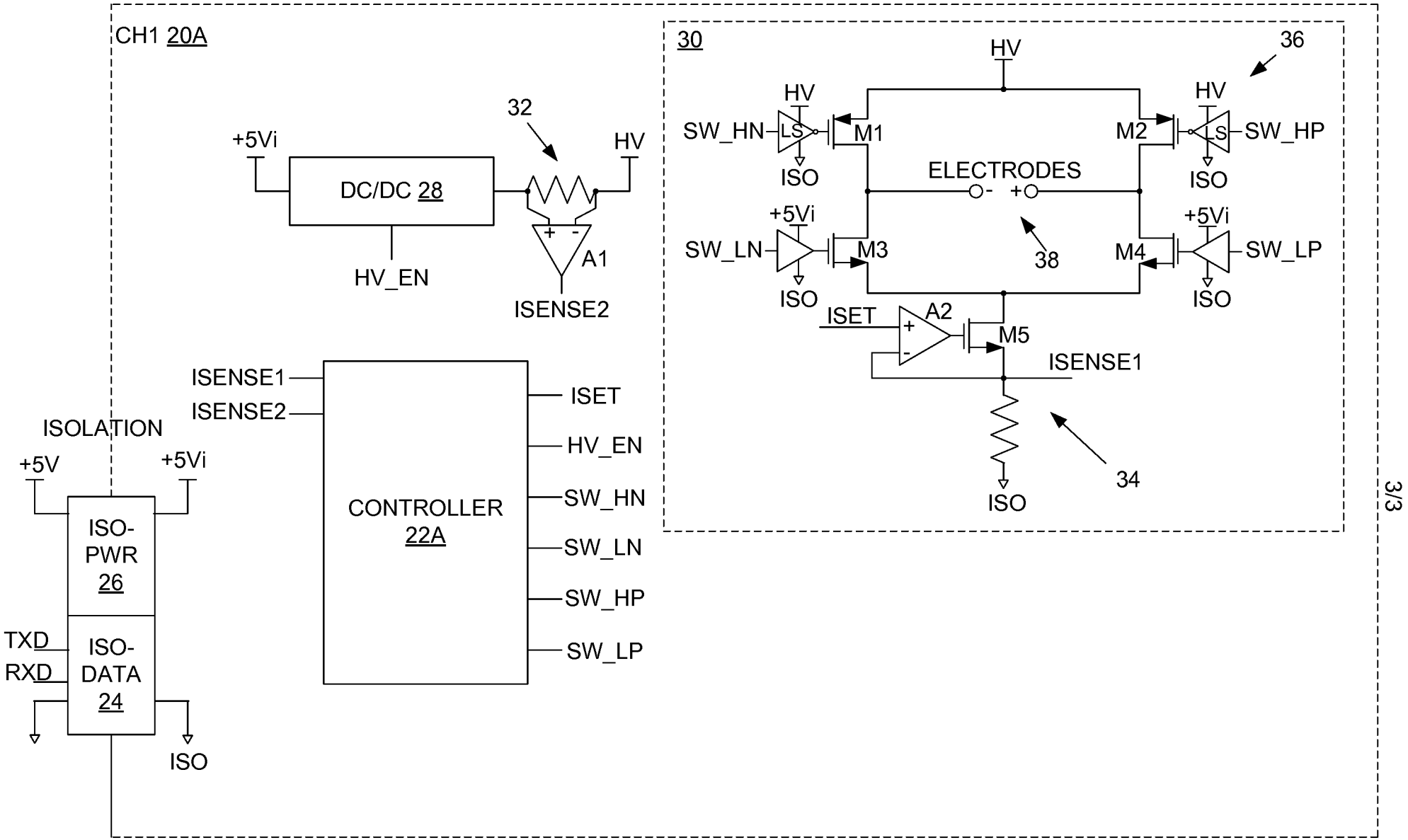
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FIG. 3