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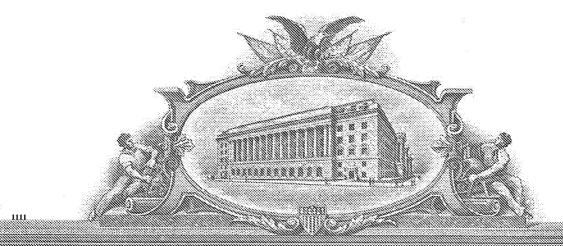
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APPLICATION NUMBER: 62/772,284 FILING DATE: November 28, 2018

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Application Date (	Chart 27 CEE	1 7 7 6	Attorney	Docke	et Numb	er	201810	0112	818					
Application Data S	(1.76	Application	mber											
Title of Invention ISC	OLATED NEUROS	ED NEUROSTIMULATOR CIRCUIT												
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Title of the Invention	ISOLATED	NEURO:	STIMULATO	R CIR	CUIT									
Attorney Docket Num	ber 2018ID1128	318			Small	l Enti	ty Stat	us (	Claime	ed				
Application Type	Provisional				•									•
Subject Matter	Utility													v
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Application Data Chart 27 CED 4 76			Attorney Docket Number 2018ID1			0112818		
Application Data Sheet 37 CFF		R 1./6	Application Number					
Title of Invention	ISOLATED NEURO	OSTIMULA	TOR CIRCUIT	Г				
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	2018ID112818
		Application Number	
Title of Invention	ISOLATED NEUROSTIMULA	TOR CIRCUIT	

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co	This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March
	<ul><li>16, 2013.</li><li>NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March</li><li>16, 2013, will be examined under the first inventor to file provisions of the AIA.</li></ul>

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	2018ID112818
		Application Number	
Title of Invention	ISOLATED NEUROSTIMULA	TOR CIRCUIT	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	2018ID112818
		Application Number	
Title of Invention	ISOLATED NEUROSTIMULA	TOR CIRCUIT	

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Application Data Chart 27 CED 4 70		Attorney Docket Number		2018ID1	12818						
Application Data Sheet 37 CFR 1.76			Application N	Number							
Title of Inven	ntion ISOLATED NEUROSTIMULATOR CIRCUIT										
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#### ISOLATED NEUROSTIMULATOR CIRCUIT

The present invention comprises an isolated, multi-channel stimulator circuit with a high voltage compliance range and improved performance. A cascode architecture reduces the operating voltage of the current source device and permits direct connection to the channel controller, thus allowing individual channels to be galvanically isolated from each other, improving safety and performance while minimizing component count.

### **Background**

Electrical neurostimulators are widely used in a variety of clinical and research contexts. These devices are commonly used for cortical stimulation in conjunction with an electroencephalography (EEG) system for functional mapping.

Problems or disadvantages overcome by the invention

Existing approaches to electrical stimulation have several limitations addressed by this invention. It is desirable for a stimulator to have a high compliance voltage to allow the use of high-impedance electrodes. In some cases, voltages up to 250V may be necessary. However, circuit architectures typically used for neurostimulators typically expose the main current source transistor to the full compliance voltage. Since the current source is controlled by low-voltage digital and mixed-signal circuits, this approach necessitates the use of costly and esoteric analog isolation circuitry, such as photo-MOS transistors and optical isolators. In addition to cost, analog optical isolation limits achievable stimulation bandwidth and decreases linearity and accuracy. In the present invention, high-voltage cascode transistors are used to reduce the voltage seen by the main current source transistor, permitting direct connection between the high-voltage current source and the low-voltage channel controller.

Additional complexity arises when multiple stimulation channels are used. Existing approaches typically place all of the stimulator channels in one isolation domain, which results in poorly-controlled current paths, reducing stimulation effectiveness and increasing risk to the patient. Mitigating these added risks requires significant circuit complexity and increases cost, size, and power consumption. The present invention places each stimulation channel into a dedicated isolation domain, and places the channel controller on the isolated side to eliminate the need to send analog signals across the galvanic isolation barrier. Risk to the patient is minimized, because current flow between channel circuits is not possible.

The main element(s) of the invention

The present invention comprises an isolated, multi-channel stimulator circuit. Each stimulator channel is a galvanically isolated unit comprising an isolated power source, isolated digital data link, a step-up DC/DC converter, an H-bridge current source, control circuits, and safety circuits. The H-bridge uses high-voltage switch transistors configured as cascode source followers to reduce the maximum voltage seen by the main current source to logic levels. This permits all control and supervision functions to be performed by a standard, low-cost microcontroller or FPGA with a minimum of additional interface or isolation circuitry.

#### Detailed description of how to build and use the invention

The stimulator system comprises a system controller and one or more mutually galvanically isolated stimulation channels. The system controller generates the appropriate stimulation parameters, communicates them to channel controllers, and monitors system operation and safety (for example, by monitoring current consumed by each stimulation channel and periodically polling the status of each channel controller).

A block diagram of the isolated stimulator channel circuit is shown in the preceding figure. The channel receives galvanically isolated low-voltage power and digital data and optionally timing signals thorough the block labelled "isolation". A DC/DC step-up converter converts the low voltage power to the appropriate voltage for stimulation (typically in the range of 20..250V). This DC/DC converter may employ a variable conversion ratio to allow operation with different electrode impedances and stimulation current ranges. Optionally, the ratio can be adjusted dynamically to maintain current source compliance by measuring the voltage at the drain of M5 during stimulation and adjusting the conversion ratio to maintain a sufficient compliance margin.

The current source unit comprises the switch FETs (M1, M2), cascode FETs (M3, M4), a current source FET (M5), a sense resistor (R1), and an error amplifier (A2). To generate both positive and negative currents, the switches and cascode FETs are configured as an H-bridge. For example, to produce a current from the + electrode to the – electrode, SW\_HP and SW\_LN are driven high, while SW\_LP and SW\_HN are driven low; this turns on M2 and M3 and turns off M1 and M4. ISET is driven with a voltage proportional to the desired current; the error amplifier adjusts the current through M5 so that it is equal to V(ISET)/R(R1). The cascode devices M3/M4 limit the voltage on the drain of M5 to below V(+5Vi), allowing high-speed, low-voltage devices to be used for M5 and A2, thus improving bandwidth.

Other features of this configuration include the ability to short the electrodes to either the +HV or the ISOGND rails. It is important to maintain charge balance during stimulation to prevent polarization and unwanted chemical reactions at the skin-electrode interface. Since it is not possible to guarantee perfect matching between the total charge of the positive and negative halves of the stimulation waveform, a small amount of imbalance charge will build up on the electrode capacitance after every stimulation pulse train. Shorting the electrodes between stimulation pulses is a simple and effective way of removing this charge. Shorting the electrodes to the +HV rail is also an effective way of precharging the parasitic capacitance between the isolated channel and the patient, thus avoiding artifacts and excessive current flow at the beginning of the stimulation pulse, or when switching polarity.

A channel controller block (comprising at least one processing element, such as an FPGA or MCU, and associated interface circuits) controls the operation of the stimulator channel. The primary function of the controller block is to generate a voltage proportional to the programmed current on the ISET output and to control the operation of the SW\_xx switches to generate the appropriate waveform on the patient electrodes. The main system processor communicates with the channel controller via a galvanically isolated digital interface (such as an asynchronous serial port).

The channel controller is also responsible for monitoring system status to ensure patient safety. The measured parameters may include compliance voltage (drain of M5), return current sense voltage V(ISENSE1), and the supply current sense voltage V(ISENSE2). Faults in the current source circuit will result in a mismatch between the supply and return currents and/or a mismatch between the programmed and sensed currents. Upon detection of a fault, the controller can put the circuit in a failsafe state by disabling the DC/DC converter and turning off all switches. Optionally, the system controller may shut down the isolated power supply to the faulty channel and/or disconnect the patient electrodes from the current source outputs.

To ensure safety against single faults, the controller may incorporate auxiliary safety monitoring circuits, such as watchdog timers and auxiliary processing elements. For example, the main processing unit may be an FPGA, and an auxiliary supervisor MCU may provide parallel supervision. If either processing unit detects a fault or is unable to communicate with the other unit, it may generate a fault signal and the channel put in a failsafe state.

The primary application of this invention is in the neurology field. It has direct applicability to the GTEN project in the Philips Neuro business unit, and significant applicability in a variety of new products currently being conceptualized and/or developed by Philips Neuro. The primary

application field is clinical intraoperative monitoring, functional mapping, and neurology research.	

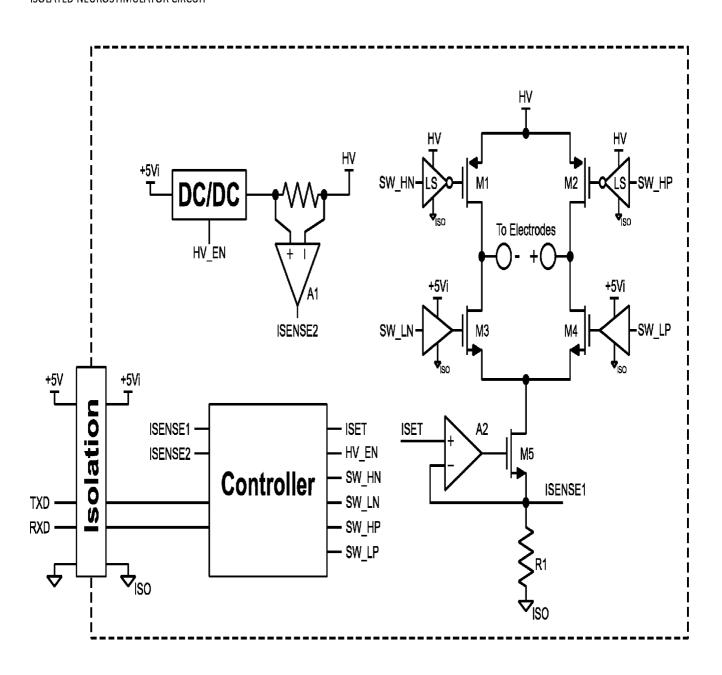


FIG. 1

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EFS ID:	34422035			
Application Number:	62772284			
International Application Number:				
Confirmation Number:	7555			
Title of Invention:	ISOLATED NEUROSTIMULATOR CIRCUIT			
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#### **New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

#### National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

### New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.