

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

To: HARRIS, Philip W. Holland & Hart LLP P.O. Box 11583 Salt Lake City, Utah 84147 USA

Date of mailing (day/month/year) 07 December 2018 (07.12.2018)
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Applicant's or agent's file reference P154WO88231	FOR FURTHER ACTION See paragraph 2 below	
International application No. PCT/US2018/047359	International filing date (day/month/year) 21 August 2018 (21.08.2018)	Priority date(day/month/year) 28 August 2017 (28.08.2017)
International Patent Classification (IPC) or both national classification and IPC G11C 16/20(2006.01)i, G11C 16/26(2006.01)i, G11C 16/04(2006.01)i, G06F 12/02(2006.01)i		
Applicant MICRON TECHNOLOGY, INC.		

1. This opinion contains indications relating to the following items:

- Box No. I Basis of the opinion
- Box No. II Priority
- Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- Box No. IV Lack of unity of invention
- Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- Box No. VI Certain documents cited
- Box No. VII Certain defects in the international application
- Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea Facsimile No. +82-42-481-8578	Date of completion of this opinion 07 December 2018 (07.12.2018)	Authorized officer BYUN, Sung Cheal Telephone No. +82-42-481-8262
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WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US2018/047359

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :
 - the international application in the language in which it was filed
 - a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
2. This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))
3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:
 - a. forming part of the international application as filed:
 - in the form of an Annex C/ST.25 text file.
 - on paper or in the form of an image file.
 - b. furnished together with the international application under PCT Rule 13ter.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
 - c. furnished subsequent to the international filing date for the purposes of international search only:
 - in the form of an Annex C/ST.25 text file (Rule 13ter.1(a)).
 - on paper or in the form of an image file (Rule 13ter.1(b) and Administrative Instructions, Section 713).
4. In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2018/047359

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	<u>1-62</u>	YES
	Claims	<u>NONE</u>	NO
Inventive step (IS)	Claims	<u>3-5,18-24,28-31,38-40,47-51,55-58</u>	YES
	Claims	<u>1-2,6-17,25-27,32-37,41-46,52-54,59-62</u>	NO
Industrial applicability (IA)	Claims	<u>1-62</u>	YES
	Claims	<u>NONE</u>	NO

2. Citations and explanations :

Reference is made to the following documents:

- D1: US 2012-0127807 A1 (FEDERICO PIO) 24 May 2012
- D2: US 2016-0155507 A1 (MICRON TECHNOLOGY, INC.) 02 June 2016
- D3: US 2012-0327728 A1 (JACOB ROBERT ANDERSON et al.) 27 December 2012
- D4: US 2014-0092687 A1 (SPANSION LLC) 03 April 2014
- D5: US 2017-0186486 A1 (INTEL CORPORATION) 29 June 2017

2.1 Novelty and Inventive Step (PCT Article 33(2) and (3))

2.1.1 Independent Claim 1

Claim 1 is an independent claim and relates to a method.

D1, which is considered to be the closest prior art to the subject matter of claim 1, discloses a method comprising receiving an instruction including a command to operate at a location in a memory, and at least one operating, wherein a memory instruction may include a READ command, an address, and an operating parameter VREAD parameter (see paragraph [0038] and claim 1 in D1).

The subject matter of claim 1 differs from D1 in executing a part of a read command on at least one portion of a memory array based at least in part on identifying the at least one portion of the memory array. However, the different feature can be merely a matter of design option in view of the feature of D1 considering affecting a physical operating condition of peripheral circuitry in said memory based, at least in part, on said at least one operating parameter, wherein a microcontroller 135 may interpret the command and use the operating parameter information to execute the memory instruction (see paragraph [0022], claim 1 and figure 1 in D1). Accordingly, claim 1 would have been obvious over D1. Therefore, claim 1 is

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novel under PCT Article 33(2), but lacks an inventive step under PCT Article 33(3).

2.1.2 Dependent Claims 2-17

Claims 2-17 are directly or indirectly dependent on claim 1.

The additional feature of claim 2 can be merely a matter of design option in view of the feature of D1 considering that one or more operating parameters may accompany read data resulting from execution of a read command (see paragraph [0020] in D1).

The additional feature of claim 3 differs from these prior art documents in increasing a voltage applied to all word lines associated with the at least one portion to a first voltage above a threshold voltage of memory cells of the at least one portion, and increasing a voltage applied to at least one gate of at least one select gate device of the at least one portion to a second voltage above a second threshold voltage of the at least one select gate device. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination.

Claim 4 is dependent on claim 3.

The additional feature of claim 5 differs from these prior art documents in that a transient state of memory cells of the at least one portion includes retaining a word line to a channel potential difference of the memory cells at a level that is lower than a voltage of a source, a drain, a bit line, or a combination thereof of the memory cells after executing the part of the read command. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination.

The additional feature of claim 6 can be merely a matter of design option in view of the feature of D1 considering that an operating parameter may also represent a current value (e.g., for use in flash or floating gate memories) or other physical quantity, such as a resistance value (e.g., for use in PCM), or a time duration or delay (see paragraph [0022] in D1).

The additional feature of claim 7 can be merely a matter of design option in view of the feature of D1 considering that a memory device may comprise a memory array to store addressable data (see paragraph [0021] in D1).

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The additional feature of claim 8 can be merely a matter of design option in view of the feature of D1 considering that an operating parameter included in a memory instruction may be received by a memory device as a digital or analog value or as a code to be interpreted by the memory device to determine one or more physical operating conditions and/or operating modes of the memory device (see paragraph [0016] in D1).

The additional features of claims 9-11 can be merely matters of design option in view of the feature of D1 considering that in addition to including a command and possibly an address descriptive of the memory location, the memory device may receive such a memory instruction that includes a command to operate at a memory location (see paragraph [0038] in D1).

The additional feature of claim 12 can be merely a matter of design option in view of the feature of D1 considering that the memory device may be operated using a memory instruction and may comprise volatile or nonvolatile memory including flash NAND (see paragraph [0015] in D1).

The additional feature of claim 13 can be merely a matter of design option in view of the feature of D1 considering initiating said instruction to said memory controller to provide access to said array of memory cells (see claim 17 in D1).

The additional features of claims 14-17 are known from the combined features of D1 considering receiving an instruction including a command to operate at a location in a memory, and at least one operating parameter, and affecting a physical operating condition of peripheral circuitry in said memory based, at least in part, on said at least one operating parameter, wherein a microcontroller 135 may interpret the command and use the operating parameter information to execute the memory instruction (see paragraph [0022], claim 1 and figure 1 in D1) and D2 considering receiving a command for the access operation, and performing an access operation on a memory device using trims corresponding to trim settings, wherein setting parameters are to be utilized by the memory device to perform the access operation on the grouping of memory cells in response to the trim settings (see paragraph [0049], claims 1-2 and figure 7 in D2).

Accordingly, it would be obvious to a person skilled in the art to arrive at claims 2 and 6-13 over D1, and to combine the disclosures of D1 and D2 to arrive at claims 14-17.

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Therefore, claims 2 and 6-17 are novel under PCT Article 33(2), but lack an inventive step under PCT Article 33(3), and claims 3-5 meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.3 Independent Claim 18

The subject matter of claim 18 differs from these prior art documents in that a method in claim 18 comprises applying, to all word lines associated with at least one portion, a voltage that increases to a first voltage above a threshold voltage of memory cells of the at least one portion based at least in part on initiating, applying, to at least one gate of at least one select gate device of the at least one portion, a voltage that increases to a second voltage above a second threshold voltage of the at least one select gate device based at least in part on the initiating, and setting a node of the at least one portion to a third voltage based at least in part on the initiating. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 18 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.4 Dependent Claims 19-24

Claims 19-24 are directly or indirectly dependent on claim 18 and therefore meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.5 Independent Claim 25

Claim 25 relates to an apparatus. As the features of independent claim 25 essentially correspond to those of claim 1 except for the category of invention, the same reasoning as in claim 1 applies to claim 25. Therefore, claim 25 is novel under PCT Article 33(2), but lacks an inventive step under PCT Article 33(3) as being obvious over D1.

2.1.6 Dependent Claims 26-27

Claims 26-27 are dependent on claim 25.

The additional feature of claim 26 can be merely a matter of design option in view of the feature of D1 considering that in addition to including a command and possibly an address descriptive of the memory location, the memory device may receive such a memory instruction that includes a command to operate at a memory location (see paragraph [0038] in D1).

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The additional feature of claim 27 essentially corresponds to that of claim 13. Accordingly, the same reasoning as in claim 13 applies to claim 27.

Accordingly, it would be obvious to a person skilled in the art to arrive at claims 26-27 over D1. Therefore, claims 26-27 are novel under PCT Article 33(2), but lack an inventive step under PCT Article 33(3).

2.1.7 Independent Claim 28

Claim 28 relates to an apparatus. As the features of independent claim 28 essentially correspond to those of claim 18 except for the category of invention, the same reasoning as in claim 18 applies to claim 28. Therefore, claim 28 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.8 Dependent Claims 29-31

Claims 29-31 are dependent on claim 28 and therefore meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.9 Independent Claim 32

Claim 32 is an independent claim and relates to a method.

D1, which is considered to be the closest prior art to the subject matter of claim 32, discloses a method comprising:

receiving an instruction including a command to operate at a location in a memory, and at least one operating parameter, wherein a memory instruction may include a READ command, an address, and an operating parameter VREAD parameter (see paragraph [0038] and claim 1 in D1); and

initiating an instruction to a memory controller to provide access to an array of memory cells (see claim 17 in D1).

The subject matter of claim 32 differs from that of D1 in executing a truncated read operation concurrently on a plurality of portions to set the plurality of portions in a first state based at least in part on identifying the plurality of portions. However, the different feature can be merely a matter of design option in view of the combined features of D1 considering affecting a physical operating condition of peripheral circuitry in said memory based, at least in

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part, on said at least one operating parameter, wherein a microcontroller 135 may interpret the command and use the operating parameter information to execute the memory instruction (see paragraph [0022], claim 1 and figure 1 in D1), and D3 which is in the same technical field as D1, considering that a command latch decoder 204 may generate internal signals that are derived from command signals each may receive, wherein the received signals may be shifted and/or truncated (see paragraph [0029] and figure 2 in D3). Accordingly, it would be obvious to a person skilled in the art to combine the disclosures of D1 and D3, thereby arriving at claim 32. Therefore, claim 32 is novel under PCT Article 33(2), but lacks an inventive step under PCT Article 33(3).

2.1.10 Dependent Claims 33-35

Claims 33-35 are dependent on claim 32.

The additional features of claims 33-34 can be merely matters of design option in view of the feature of D1 considering receiving a memory instruction that includes a command to operate at a memory location, wherein the memory instruction may include a READ command, an address, and an operating parameter VREAD, and modifying one or more physical operating conditions in response to receiving the operating parameter (see paragraph [0038] and figure 5 in D1).

The additional feature of claim 35 is known from the combined features of D1 considering receiving a memory instruction, wherein the memory instruction may include a READ command, an address, and an operating parameter VREAD, and modifying one or more physical operating conditions in response to receiving the operating parameter (see paragraph [0038] and figure 5 in D1) and D3 considering that a command latch decoder 204 may generate internal signals that are derived from the command signals each may receive, wherein the received signals may be shifted and/or truncated (see paragraph [0029] and figure 2 in D3).

Accordingly, it would be obvious to a person skilled in the art to combine the disclosures of D1 and D3, thereby arriving at claims 33-35. Therefore, claims 33-35 are novel under PCT Article 33(2), but lack an inventive step under PCT Article 33(3).

2.1.11 Independent Claim 36

Claim 36 relates to an apparatus. As the features of independent claim 36 essentially

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correspond to those of claim 1 except for the category of invention, the same reasoning as in claim 1 applies to claim 36. Therefore, claim 36 is novel under PCT Article 33(2), but lacks an inventive step under PCT Article 33(3) as being obvious over D1.

2.1.12 Dependent Claims 37-46

Claims 37-46 are directly or indirectly dependent on claim 36.

The additional features of claims 37-41, 42-44, and 45-46 essentially correspond to those of claims 2-6, 8-10, and 13-14, respectively. Accordingly, the same reasoning as in claims 2-6, 8-10, and 13-14 applies to claims 37-46. Therefore, claims 37 and 41-45 are novel under PCT Article 33(2), but lack an inventive step under PCT Article 33(3) as being obvious over D1, claim 46 is novel under PCT Article 33(2), but lacks an inventive step under PCT Article 33(3) as being obvious over D1 in view of D2, and claims 38-40 meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.13 Independent Claim 47

Claim 47 relates to an apparatus. As the features of independent claim 47 essentially correspond to those of claim 18 except for the category of invention, the same reasoning as in claim 18 applies to claim 47. Therefore, claim 47 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.14 Dependent Claims 48-51

Claims 48-51 are dependent on claim 47 and therefore meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.15 Independent Claim 52

Claim 52 relates to an apparatus. As the features of independent claim 52 essentially correspond to those of claim 25 except for the category of invention, the same reasoning as in claim 25 applies to claim 52. Therefore, claim 52 is novel under PCT Article 33(2), but lacks an inventive step under PCT Article 33(3) as being obvious over D1.

2.1.16 Dependent Claims 53-54

Claims 53-54 are dependent on claim 52.

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The additional features of claims 53-54 essentially correspond to those of claims 26-27, respectively. Accordingly, the same reasoning as in claims 26-27 applies to claims 53-54. Therefore, claims 53-54 are novel under PCT Article 33(2), but lack an inventive step under PCT Article 33(3) as being obvious over D1.

2.1.17 Independent Claim 55

Claim 55 relates to an apparatus. As the features of independent claim 55 essentially correspond to those of claim 18 except for the category of invention, the same reasoning as in claim 18 applies to claim 55. Therefore, claim 55 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.18 Dependent Claims 56-58

Claims 56-58 are dependent on claim 55 and therefore meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2.1.19 Independent Claim 59

Claim 59 relates to an apparatus. As the features of independent claim 59 essentially correspond to those of claim 32 except for the category of invention, the same reasoning as in claim 32 applies to claim 59. Therefore, claim 59 is novel under PCT Article 33(2), but lacks an inventive step under PCT Article 33(3) as being obvious over D1 in view of D3.

2.1.20 Dependent Claims 60-62

Claims 60-62 are dependent on claim 59.

The additional features of claims 60-62 essentially correspond to those of claims 33-35, respectively. Accordingly, the same reasoning as in claims 33-35 applies to claims 60-62. Therefore, claims 60-62 are novel under PCT Article 33(2), but lack an inventive step under PCT Article 33(3) as being obvious over D1 in view of D3.

2.2 Industrial Applicability (PCT Article 33(4))

Claims 1-62 are industrially applicable under PCT Article 33(4).