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PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/EP2018/064039	29.05.2018	02.06.2017

International Patent Classification (IPC) or both national classification and IPC
INV. G01F23/284 G01S13/88

Applicant
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1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/EP2018/064039

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

   a. ☐ forming part of the international application as filed:

      ☐ in the form of an Annex C/ST.25 text file.

      ☐ on paper or in the form of an image file.

   b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

   c. ☐ furnished subsequent to the international filing date for the purposes of international search only:

      ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).

      ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	2, 3, 5-7, 15-19
	No:	Claims	1, 4, 8-14
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-19
Industrial applicability (IA)	Yes:	Claims	1-19
	No:	Claims	

2. Citations and explanations

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

1 **Re Item V**

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1.1 Reference is made to the following documents:

D1 Brian Ginsburg ET AL: "Fluid-level sensing using 77-GHz millimeter wave",
, 3 May 2017 (2017-05-03), XP055499812,
Retrieved from the Internet:
URL:http://www.ti.com/lit/wp/spyy004/spyy004.pdf
[retrieved on 2018-08-14]

D2 US 2008/278145 A1 (WENGER FABIAN [SE]) 13 November 2008 (2008-11-13)

D3 Anonymous: "MSP Low-Power Microcontrollers",
, 23 March 2016 (2016-03-23), XP055500341,
Retrieved from the Internet:
URL:http://www.ti.com/lit/sg/slab034ad/slab034ad.pdf
[retrieved on 2018-08-16]

D4 US 2004/143769 A1 (DENG XIAOWEI [US] ET AL) 22 July 2004 (2004-07-22)

D5 US 2006/268648 A1 (DANG LUAN A [US] ET AL) 30 November 2006 (2006-11-30)

D6 US 2015/092477 A1 (CHIOU LIH-YIH [TW] ET AL) 2 April 2015 (2015-04-02)

1.2 The present application does not meet the criteria of Article 33(2) PCT, because the subject-matter of claim 1 is not new.

1.2.1 D1 (references in parentheses applying to this document, see pages 2-4, 6-8; Figs. 1, 2, 3) discloses:

a radar level gauge (see title) for determining a filling level of a product in a tank (see tank-level probing radar, page 2, Introduction), said radar level gauge comprising:
- transceiver circuitry configured to generate and transmit an electromagnetic

transmit signal, and to receive an electromagnetic return signal (see Fig. 1 on page 3; "three transmit and four receive chains", end of page 3);
- processing circuitry (see Fig. 1; ARM Cortex-R4F processor, page 3) connected to the transceiver circuitry and configured to determine the filling level based on a relationship between the transmit signal and the return signal,
- a temporary energy store (see Fig. 3 and paragraph above it on page 7) for storing energy from an energy source (the continuous power from the 4-20 mA control loop is not sufficient for the peak power consumption of the IWR1443 sensor; see page 8) selected as at least one of: a power-limited power interface (see 4-20 mA control loop, on page 7, first paragraph) and a localized energy-limited energy source,
- power management circuitry (see Fig. 3 on page 7) configured to distribute power from the energy store to said transceiver circuitry and said processing circuitry, and
- communication circuitry (see Fig. 1 on page 3; also page 7, top of right column) connected to receive measurement data from the processing circuitry and to communicate said measurement data externally of the radar level gauge, wherein the processing circuitry includes:
a volatile high-speed working memory (see RAM, for example R4F program RAM on pages 4, 6; Table 1; Fig. 2),
a first processing unit (ARM Cortex-R4F processor; see Fig. 1, page 3) connected to said volatile high-speed working memory, said first processing unit having an active mode in which the first processing unit is turned on and accesses the working memory, and an inactive mode where said first processing unit is turned off off (the processor is powered off between measurements, see page 7, second and fourth paragraph),
memory loading circuitry (see DMA in Figs. 1, 2; pages 3, 6), separate from said first processing unit, configured to transfer software code from a non-volatile memory (see serial Flash, page 7 fourth paragraph; Fig. 3) into said volatile high-speed working memory while said first processing unit is in inactive mode (see page 7, fourth paragraph; Fig. 3), and
an auxiliary power connection configured to provide power only to said volatile high-speed working memory and said memory loading circuitry (see power management in Fig. 3, page 7, in conjunction with page 6, right column, second paragraph).

Therefore the subject-matter of claim 1 is not new in the sense of Article 33(2) PCT.

1.2.2 Moreover, the subject-matter of claim 1 lacks novelty (Article 33(2) PCT) with respect to D2 (see §[0028]-[0041]; Figs. 1-3), which discloses a radar level gauge (1 in Fig. 1; §[0028]), comprising: transceiver circuitry (11 in Fig. 2; §[0032]), processing circuitry (12; §[0032]), a temporary energy store (26; §[0038]); with power supply interface 27), power management circuitry (implicitly comprised in arbitration logic 22; see §[0037]-[0038]), communication circuitry (15; §[0033]), a volatile high-speed working memory (see RAM 14, 18), a first processing unit (13) with an active mode and an inactive mode (see sleep mode in §[0041]), memory loading circuitry (see DMA in §[0039]-[0040]), non-volatile memory (for example 21; see §[0039] and an auxiliary power connection for powering said volatile high-speed working memory and the memory loading circuitry (see arbitration logic 22 controlling the sleep timer processes 23, 24 (sleep mode); §[0041]).

1.3 The present application does not meet the criteria of Article 33(3) PCT, because the subject-matter of claim 15 does not involve an inventive step.

1.3.1 D1 (see pages 2-4, 6-8; Figs. 1, 2, 3) may be regarded as being the prior art closest to the subject-matter of claim 15, and discloses:

a method in a radar level gauge for measuring a distance to a surface of a product kept in a tank (see tank-level probing radar on page 2, Introduction), said method comprising:
arranging in said radar level gauge:
a non-volatile memory (see serial Flash; page 7, right column; Fig. 3) having a first random data access time;
a volatile working memory (RAM; for example R4F program RAM on pages 4, 6; Table 1; Fig. 2) having a second random data access time being a fifth (1/5) or less of said first random data access time (implicitly, since modern RAM implementations have much shorter random data access times that Flash memory); and having at least a working memory operational mode ~~and a working memory power saving mode, said power saving mode enabling saving at least 95% of the power requirement of said operational mode while retaining current working memory contents therein~~;
a first processing unit (see ARM Cortex-R4F processor; see Fig. 1, page 3) having at least a first processing unit operational mode and a first processing unit power saving mode, said power saving mode enables saving at least 90% of the power requirement of said first processing unit operational mode (the processor is powered down; see page 7, second and fourth paragraph);

said method comprising:
transferring software code from said non-volatile memory to said volatile working memory (see page 7, fourth paragraph),
applying a cyclic measuring scheme wherein a measurement cycle includes an energy accumulation phase, a measurement phase, a communication phase (see page 7, fourth paragraph; also page 8);
said energy accumulation phase comprising:
setting ~~said working memory power saving mode and~~ said first processing unit power saving mode;
drawing energy, preferably that needed for performing a complete measurement cycle, from an energy source selected as at least one of: a power-limited power interface (see 4-20 mA control loop, on page 7, first paragraph) and a localized energy-limited energy source;
storing intermediately the energy in a temporary power store (see Fig. 3 and paragraph above it on page 7; also page 8), which enables discharge of energy at a higher rate than, preferably at least ten times, that of said energy source (implicitly, since the continuous power from the 4-20 mA control loop is not sufficient for the peak power consumption of the IWR1443 sensor; see page 8);
said measurement phase comprising:
transmitting an electromagnetic transmit signal, via a signal propagation device, towards the surface (see transmitters in Fig. 1; page 3);
receiving an electromagnetic return signal, via said signal propagation device, reflected at said surface (see receivers in Fig. 1; page 3);
determining said distance in said first processing unit, based on a relation between said transmit signal and said return signal, by executing said software code stored in the working memory (see pages 7-8);
said communication phase comprising:
communicating externally of said radar level gauge a measurement value indicative of said distance, typically involving any change to a most up to date measurement value (see page 7, right column; also 4-20 mA control loop, Fig. 3),
wherein the step of transferring software code from said non-volatile memory to said volatile working memory includes:
setting said first processing unit in its first processing unit power saving mode, providing operating power to a memory loading circuitry (see DMA in Figs. 1 and 2; pages 3, 6), separate from said first processing unit,
using said memory loading circuitry to transfer said software code from the

non-volatile memory into said volatile working memory while said first processing unit is in said first processing unit power saving mode (see page 7, fourth paragraph, Fig. 3; in conjunction with page 6, right column, second paragraph).

1.3.2 The subject-matter of claim 15 therefore differs from this known method in that:
- the volatile working memory has a working memory power saving mode, said power saving mode enabling saving at least 95% of the power requirement of said operational mode while retaining current working memory contents therein; and
- during the energy accumulation phase the working memory is set to the power saving mode.

1.3.3 The problem to be solved by the present invention may therefore be regarded as minimizing power consumption between measurements.

1.3.4 The solution proposed in claim 15 of the present application cannot be considered as involving an inventive step (Article 33(3) PCT) for the following reasons:
The solution of providing a volatile high-speed working memory having a memory preserving low power mode is rendered obvious by D1, which mentions a "low-leakage sleep mode" (see page 7, second paragraph). Even if the device of D1 does not include this feature, it is immediately clear that it can be added to solve the aforementioned problem. Because this feature is well known in the art (as a solution to a common design problem), see for example D3 (selectable RAM retention on page 5) or D4 (abstract) or D5 (abstract) or D6 (abstract), it is obvious to the person skilled in the art how to implement it.

1.3.5 Therefore the subject-matter of claim 15 does not involve an inventive step in the sense of Article 33(3) PCT.

1.3.6 Moreover, the subject-matter of claim 15 does not involve an inventive step (Article 33(3) PCT) in view of D2 (see §[0028]-[0041]; Figs. 1-3), for the same reasons as above. The subject-matter of claim 15 differs from the disclosure of D2 also in that a volatile working memory with content preserving low power mode is provided, therefore the same analysis as with respect to D1 (see sections 1.3.2 - 1.3.4 above) also applies to D2.

1.4 Dependent claims 4, 8-13, 14 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty (Article 33(2) PCT):
- claim 4: DMA is known from D1 (see DMA in Figs. 1 and 2; pages 3, 6) or D2 (see DMA in §[0039]);
- claim 8: see D1 ("three transmit and four receive chains", end of page 3);
- claims 9 and 10: an integrated circuit is disclosed by D1 (see "highly integrated single chip" on end of page 3) or D2 (§[0039]);
- claims 11 and 12: the frequency range is known from D1 (see 77-81 GHz on page 5, top of right column);
- claim 13: see D1 (4-20 mA control loop on page 7, Fig. 3);
- claim 14: see D2 (battery in §[0038]).

1.5 Dependent claims 2, 3, 5-7, 16-19 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step (Article 33(3) PCT, for the following reasons:

1.5.1 Claims 2 and 17: Memory verification is a commonly applied feature in modern sensor integrated circuits (as the one shown in D2 (page 5)). Moreover, see D6 (abstract; data loss detector). It would be obvious to the person skilled in the art, namely when the same result is to be achieved, to apply this feature with corresponding effect to a radar level gauge according to D1.

1.5.2 Claims 3, 16, 18: The same reasoning as in section 1.3.4 applies. The subject-matter is rendered obvious by D1, which mentions a "low-leakage sleep mode" (see page 7, second paragraph). Even if the device of D1 does not include this feature, it is immediately clear that it can be added to minimize the power consumption between measurements. Since this feature is well known in the art (as a solution to a common design problem), see for example D3 (selectable RAM retention on page 5) or D4 (abstract) or D5 (abstract) or D6 (abstract), it is obvious to the person skilled in the art how to implement it.

1.5.3 Claim 5: A software implemented boot-loader is rendered obvious by the teachings of D1 (see page 7, fourth paragraph).

1.5.4 Claims 6 and 7: Dividing software code into smaller portions for transfer in limited power circumstances is well known in the art; moreover, see D5 (abstract; individually addressable data bits in SRAM). This additional feature,

as well as a required energy of 20 mW (claim 7), are obvious design options that the person skilled in the art would include in the device of D1, according to the circumstances, without exercising inventive skill.

1.5.5 Claim 19: Since no additional features are defined, see reasoning above, in particular relating to claim 15 (sections 1.3.1 - 1.3.6).

2 Re Item VII

Certain defects in the international application

2.1 Independent claims are not in the two-part form in accordance with Rule 6.3(b) PCT, with those features known in combination from the prior art being placed in the preamble (Rule 6.3(b)(i) PCT) and the remaining features being included in the characterising part (Rule 6.3(b)(ii) PCT).

2.2 The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

2.3 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in D1 and D2 is not mentioned in the description, nor are these documents identified therein.

3 Re Item VIII

Certain observations on the international application

3.1 The application does not meet the requirements of Article 6 PCT, because claim 16 is not clear.

3.2 Claim 16 is unclear because it depends on itself. It is understood that it was meant to be dependent on claim 15, and is interpreted as such.