STABLE THRESHOLD SWITCHING MATERIALS FOR SELECTORS OF RESISTIVE MEMORIES

BACKGROUND

[0001] Non-volatile memory is computer memory that can store information even when not powered. Types of non-volatile memory may include resistive RAM (random access memory) (RRAM or ReRAM), phase change RAM (PCRAM), conductive bridge RAM (CBRAM), ferroelectric RAM (F-RAM), etc.

[0002] Resistance memory elements, such as resistive RAM, or ReRAM, can be programmed to different resistance states by applying programming energy. After programming, the state of the resistive memory elements can be read and remains stable over a specified time period. Large arrays of resistive memory elements can be used to create a variety of resistive memory cells, including non-volatile solid state memory, programmable logic, signal processing, control systems, pattern recognition devices, and other applications. Examples of resistive memory devices include valence change memory and electrochemical metallization memory, both of which involve ionic motion during electrical switching and belong to the category of memristors.

[0003] Memristors are devices that can be programmed to different resistive states by applying a programming energy, for example, a voltage or current pulse. This energy generates a combination of electric field and thermal effects that can modulate the conductivity of both non-volatile switch and non-linear select functions in a memristive element. After programming, the state of the memristor can be read and remains stable over a specified time period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Features of examples of the present disclosure will become apparent by reference to the following detailed description and drawings, in which like reference numerals correspond to similar, though perhaps not identical, components. For the sake of brevity, reference numerals or features having a previously described function may or may not be described in connection with other drawings in which they appear.

[0005] Fig. 1A, on coordinates of log current (I) and voltage (v), is a plot of a log I-V curve for a selector having an initial amorphous that, after forming, becomes a crystallized state, according to an example.

[0006] Fig. 1B, on coordinates of log current (I) and voltage (v), is a plot of a log I-V curve for a selector having an initial amorphous state that switches without forming and remains in an amorphous state, according to an example.

[0007] Fig. 2A is a cross-sectional view of a selector useful in 2D crossbar arrays, according to an example.

[0008] Fig. 2B is a cross-sectional view of the selector useful in 3D crossbar arrays, also known as 3D RRAM, according to an example.

[0009] Fig. 3A is a perspective view of a 2D crossbar memory array, according to an example.

[0010] Fig. 3B is a cross-sectional view of a 3D crossbar memory array, according to an example.

DETAILED DESCRIPTION

[0011] Reference is made now in detail to specific examples, which illustrate the best mode presently contemplated by the inventor for practicing examples of the present disclosure. Alternative examples are also briefly described as applicable.

[0012] Resistive memories may be suitable for persistent memory applications that require short read/write latencies. A crossbar arrangement of the resistive memory element without an access transistor at each cross point may be important for high density integration. In a crossbar arrangement of memory elements, a selector device may be employed for each cross point to prevent leakage current during read/write

operations. Usually, a selector device has two electrodes and one of the electrodes is connected to a memory element.

[0013] Threshold switches may be very promising candidates for such selector devices, since they evidence high resistances when the applied voltage is below the threshold voltage while the resistance decreases abruptly when it reaches the threshold voltage. The high resistance may be recovered when the applied voltage is removed, which differentiates the threshold switches from nonvolatile memory elements.

[0014] An example of a threshold switch may be an NbO_2 (or VO_2) switch, which can be made by BEOL (back end of line) processes only. A similar example is an Ovonic Threshold Switch (OTS) – a chalcogenide material with a similar composition to phase change memory materials. It is believed that NbO_2, VO_2, and OTS work in a same way – a voltage applied to the device results in a current, the current flowing through the device heats up the device, the current increases as the internal temperature rises, the increased current generates more heat, and it goes into a positive feedback cycle. When the current increases faster than the heat dissipation at a certain applied voltage, it goes into a thermal runaway and the current increases to a very high value until some other mechanism stops the increase. The high current (or the low resistance) is maintained until the current is lowered below a certain value (a holding current). Once the current is lowered below the holding current, the device gets cooled and the internal temperature becomes too low to maintain the thermal runaway, when the high resistance is recovered. The thermal runaway may result in a very high internal temperature, which in many cases may make the initially amorphous device crystallized at the first few turn-on events. The phase change may result in changes in many material properties, including the subthreshold resistance and the threshold voltage.

[0015] The materials that show high subthreshold resistances may be made amorphous but may form crystalline phases in the first few switching cycles, as described above. This crystallization usually decreases the subthreshold resistance significantly, and the devices' capability to block the leakage current as selectors may

be compromised. Fig. 1A depicts a semi-log plot of I-V (log in I) for such a system, shown as switching Curve 100. The plot is from the NbO_2 system. Portion 102 depicts the initial OFF state, in which the selector is amorphous. A further increase in voltage (the threshold voltage) results in an abrupt increase in current, resulting in switching and crystallization, as shown by portion 104. The abrupt switch leads to a formed ON state, in which the material is crystallized, as shown by portion 106. Reversing the voltage leads to an abrupt decrease in current and to a formed OFF state, in which the material remains crystallized, as shown by portion 110. The current for portion 110 is seen to be above the initial OFF state, and the difference, indicated by arrow 112, is the increase in leakage current. As the voltage is increased again after the forming step, the current increases following portion 110. When voltage reaches a new threshold voltage, which is lower than the initial threshold voltage, the current increases abruptly as shown by portion 108, then follows portion 106.

[0016] Another issue with threshold switches is that the threshold voltage may be reduced during the forming cycle. A forming cycle may require an initial irreversible forming step to enable the subsequent reversible resistance switching to be possible. This forming step may require a large voltage and may lead to variance from device to device. In addition, the high probability of forming failure may result in a low switchable device yield.

[0017] To set the later threshold voltage to a desired value, the devices may be designed such that the initial threshold voltage is much higher, considering the decrease after the forming step. The maximum voltage the driving circuits may be capable of handling also may be higher just because of the forming step, which will be used only a few times at initialization. The increase in operating voltage may require unnecessarily larger transistors to be used in all the driving circuits, which may result in large area and/or cost penalties. Thus, it has been highly desirable from a technological standpoint to eliminate the forming step.

[0018] There have apparently been no published solutions that describe eliminating the forming step in threshold switches. Eliminating the forming step could reduce or even eliminate the leakage current.

[0019] In prior unpublished work, it has been shown that the forming can be avoided by adding oxygen buffer layers next to the threshold switching layer, but the initial subthreshold resistance is decreased because of reduction by the oxygen buffer layer.

[0020] The present inventors have unexpectedly discovered that providing the threshold switching materials with a component that stabilizes amorphous phases may enable the forming to be avoided. Threshold switching materials usually show a forming behavior, as indicated above, in which the subthreshold resistance increases significantly after the first switching event. The deterioration can be avoided by keeping the material amorphous. This may be done by incorporating an amorphous stabilizing component into the threshold switching material. The resulting amorphous alloys may retain the initial high resistance even after repeated switching cycles.

[0021] In resistive memory switching technology, a selector may be placed in series with a resistive memory switch, such as a memristor. The structure of such a combination may be electrode/selector/electrode/resistive memory switch/electrode. In a crossbar, the outer electrodes may be connected to column and row drivers, while the middle electrode floats. As used herein, a memory cell, or memory device, is a combination of a memory element and a selector. The memory element generally may be a resistive memory element. In some examples, the resistive memory element may be a memristor.

[0022] In accordance with the teachings herein, a stable threshold switching material for selectors employed in resistive memories is provided. The material may be amorphous and may have a composition given by $(V, Nb)_{1-x}(Si, Hf, W)_xO_y$, where $0 < x < 1$ and y is within a range of 1.5 to 3. As used herein, "stable" in the context of a threshold switching material means that the characteristics of a device are maintained substantially unchanged over the life of the device.

[0023] VO_x and NbO_x may show threshold switching behavior and have been explored as selectors in resistive memories. Amorphous films of these materials may be formed when they are deposited at a low temperature. Due to the high mobilities of the constituent metal atoms and oxygen atoms in the films, they may tend to crystallize

during substantial motion of the atoms under a high electric field. However, they may become resistant to crystallization if those materials are alloyed with components that form a strong bond with an oxygen atom, such as Si, Hf, W, etc. These alloys may also evidence higher resistance, which may improve the selector performance. Examples of materials that may be suitably employed in the practice of the teachings herein may include $(V, Nb)_{1-x}(Si, Hf, W)_xO_y$, where $0 < x < 1$ and y is within a range of 1.5 to 3.

[0024] An example of a suitable amorphous material that may be suitably employed is an $Nb_{X-1}Si_xO_y$ alloy, where x is within a range of 0.01 to 0.9 and y is within a range of 2 to 2.5. These films can be deposited by sputtering an Nb-Si alloy target with an oxygen-containing gas, such as oxygen or water vapor. An NbO_{Z1}-SiO_{Z2} alloy target can be also used with or without oxygen, where z1 is within a range of 2 to 2.5 and z2 is within a range of 2 to 3. More generally, a $(V, Nb)O_{z1}$-$(Si, Hf, W)O_{z2}$ alloy target may be employed.

[0025] The alloy films can be also deposited by Atomic Layer Deposition (ALD) and may be favored for high density integration. In this case, an Nb-containing volatile precursor such as $Nb(N(CH_3)_2)_5$ or $Nb(OCH_2CH_3)$ may be introduced to a surface with O- or OH- terminations. After the surface is saturated by the precursor molecules, the excess gas may be flushed out. The surface may then be exposed to an oxygen-containing gas such as oxygen or water vapor so that oxygen in the oxygen-containing gas can react with the Nb precursor to form NbO_Z. Then the oxygen-containing gas may be flushed out and the cycle repeated to obtain the film with a desired thickness. In an example, a desired thickness range may be about 1 nm to about 100 nm. To obtain $Nb_{X-1}Si_xO_y$ alloy films, some of the steps of introducing an Nb precursor may be replaced by one or more steps of introducing a volatile Si precursor, such as $SiH(N(CH_3)_2)$, $Si(OC_2H_5)_4$, $Si((CH_2)_3NH_2)(OC_2H_5)$, $SiCl_4$, $Si(OH)(OC(CH_3)_3)_3$, or $Si(OH)(OC(CH_3)_2(C_2H_5))_3$. Different compositions of the alloy film can be deposited by changing the portion of Nb cursor in the introducing steps that are replaced by the Si precursor.

[0026] More generally, a volatile (V, Nb) precursor may be introduced to the surface with O- or OH- terminations, excess gas flushed out, oxygen-containing gas introduced so as to form (V, Nb)O_{z1}, then a volatile (Si, Hf, W) precursor introduced, excess gas flushed out, oxygen-containing gas introduced so as to form (Si, Hf, W)O_{z2} gas, and repeating these steps so as to form (V, Nb)$_{1-x}$(Si, Hf, W)$_x$$O_y$ alloy. The values of z1 and z2 are given above. The relative amounts of (V, Nb) precursor and (Si, Hf, W) precursor may be varied as needed to obtain a desired ratio of (V, Nb) to (Si, Hf, W).

[0027] Fig. 1B depicts a semi-log plot of I-V (log in I) for such a system, shown as switching Curve 150. Fig. 1B is to be compared and contrasted with Fig. 1A. Fig. 1B is intended to be a conceptual plot to illustrate a point to show substantially identical behavior before and after the first switching cycle. The plot may be for an $Nb_{1-x}Si_xO_y$ system. Portion 152 depicts the initial OFF state, which is essentially equivalent to portion 102 in Fig. 1A, in which the selector is amorphous. The absolute value of the current at a voltage of 152 may be lower than that of 102 with a same thickness. However, the thickness may be adjusted to have a desirable threshold voltage since the alloying may result in a lower subthreshold current and a higher threshold voltage for a given thickness. So the optimized current may or may not be same as 102.

[0028] A further increase in voltage (the threshold voltage) results in an abrupt increase in current, resulting in switching without forming, as shown by portion 154. The abrupt switch leads to an ON state, in which the selector remains amorphous, as shown by portion 156. Reversing the voltage leads to an abrupt decrease in current, which may retrace the same path 154 as increasing the voltage at a voltage lower than the threshold voltage of the ON-switching, and return the selector to a stable OFF state 158, in which the selector remains amorphous. OFF state 158 is seen to be substantially identical to the initial OFF state 152. Here, the current for portion 158 is seen to be essentially the same as the initial OFF state 152, and there is no change in leakage current. On the other hand, the ON-switching threshold voltage in the second and later cycles may be substantially same as the first one.

[0029] Figs. 2A-2B depict two examples of structures that employ stable threshold switching materials for selectors employed in resistive memories. In Fig. 2A, memory cell 200 including a memory element 202 and a selector 204 is depicted. The memory element 202 and the selector 204 may be arranged in series. A first electrode 206 may be in electrical contact with the selector 204, a second electrode 208 may separate the memory element 202 and the selector 204, and a third electrode 210 may be in electrical contact with the memory element 202. An insulator layer 212 may surround the memory element 202, the selector 204, and the electrodes 206, 208, 210.

[0030] The memory cell 200 may be vertically disposed, as shown here, in a 2D crossbar structure (depicted in Fig. 3A). One of the first electrode 206 or third electrode 210 may be electrically connected to bit lines in the crossbar and the other of the third electrode 210 or first electrode 206 may be electrically connected to source lines in the crossbar. Also, the memory element 202 and the selector 204 may be interchanged, so that the memory cell 202 is in electrical contact with the first electrode 206 and the selector 204 is in electrical contact with the third electrode 210.

[0031] Metal or semiconductor oxides may be employed as the memory element 202; examples include either transition metal oxides, such as tantalum oxide, titanium oxide, yttrium oxide, hafnium oxide, niobium oxide, zirconium oxide, or other like oxides, or non-transition metal oxides, such as aluminum oxide, calcium oxide, magnesium oxide, dysprosium oxide, lanthanum oxide, silicon dioxide, or other like oxides. Further examples include transition metal nitrides, such as aluminum nitride, gallium nitride, tantalum nitride, and silicon nitride. The memory element 202 may have a thickness within a range of about 1 nm to about 100 nm.

[0032] The selector 204 may be $(V, Nb)_{1-x}(Si, Hf, W)_xO_y$, where $0 < x < 1$ and y is within a range of 1.5 to 3. The selector 204 may have a thickness within a range of about 1 nm to about 100 nm. In particular, the selector 204 may be $Nb_{X-1}Si_xO_y$ alloy, where x is within a range of 0.01 to 0.9 and y is within a range of 2 to 2.5.

[0033] The first, second, and third electrodes 206, 208, 210 may be composed of any of the following materials: TiN, W, WN_2, Ta, TaN, Nb, NbN, Al, Cu, Ti, Pt, Ir, Ru,

IrO_2, RuO_2, Pd, Ni, Ag, Au, Mo, and Co. The electrodes 206, 208, 210 may each be selected from the foregoing list and may be the same or different. The thickness of each of the electrodes may be within a range of about 1 nm to about 100 nm.

[0034] The insulator layer 212 may be composed of any of the following materials: SiO_2, Al_2O_3, Ta_2O_5, TiO_2, Y_2O_3, HfO_2, Nb_2O_5, ZrO_2, CaO, MgO, Dy_2O_3, La_2O_3, and Si_3N_4, and have a thickness within a range of about 10 nm to about 1,000 nm.

[0035] In Fig. 2B, memory cell 250 including a memory element 252 and a selector 254 is depicted. The memory element 252 and the selector 254 may be arranged in series. A first electrode 256 may in electrical contact with the selector 254, a second electrode 258 may be in electrical contact both the memory element 252 and the selector 254, and a third electrode 260 may be in electrical contact with the memory element 252. An insulator layer 262 may be above and below the selector 254 and the second electrode 258 and provide a supporting surface for the memory element 252.

[0036] The memory cell 250 may be disposed, as shown here, in a 3D crossbar structure (depicted in Fig. 3B). In 3D crossbars, also known as 3D RRAM (Resistive Random Access Memory), stacks are formed of horizontal layers that each form the first electrode 256 separated by horizontal layers of insulator 262. The selector 254 may be formed in a recess 264 at the end of each first electrode layer 256. The selector 254 may be generally U-shaped, and the second electrode 258 may be formed in the bight of the U-shaped selector 254.

[0037] One of the first electrode 256 or third electrode 260 may be electrically connected to bit lines in the crossbar and the other of the third electrode 260 or first electrode 256 may be electrically connected to source lines in the crossbar. Also, the memory element 252 and the selector 254 may be interchanged, so that the memory cell, now 254, is in electrical contact with the first electrode 256 and the selector, now 252 is in electrical contact with the third electrode 260.

[0038] Metal or semiconductor oxides may be employed as the memory element 252; examples include either transition metal oxides, such as tantalum oxide, titanium oxide, yttrium oxide, hafnium oxide, niobium oxide, zirconium oxide, or other like

oxides, or non-transition metal oxides, such as aluminum oxide, calcium oxide, magnesium oxide, dysprosium oxide, lanthanum oxide, silicon dioxide, or other like oxides. Further examples include transition metal nitrides, such as aluminum nitride, gallium nitride, tantalum nitride, and silicon nitride. The memory element 252 may have a thickness within a range of about 1 nm to about 100 nm.

[0039] The selector 254 may be $(V, Nb)_{1-x}(Si, Hf, W)_xO_y$, where $0 < x < 1$ and y is within a range of 1.5 to 3. The selector 254 may have a thickness within a range of about 1 nm to about 100 nm. In an example, the selector 254 may be $Nb_{X-1}Si_xO_y$ alloy, where x is within a range of 0.01 to 0.9 and y is within a range of 2 to 2.5.

[0040] The first, second, and third electrodes 256, 258, 260 may be composed of any of the following materials: TiN, W, WN_2, Ta, TaN, Nb, NbN, Al, Cu, Ti, Pt, Ir, Ru, IrO_2, RuO_2, Pd, Ni, Ag, Au, Mo, and Co. The electrodes 256, 258, 260 may each be selected from the foregoing list and may be the same or different. The thickness of each of the electrodes may be within a range of about 1 nm to about 1,000 nm.

[0041] The insulator layer 262 may be composed of any of the following materials: SiO_2, Al_2O_3, Ta_2O_5, TiO_2, Y_2O_3, HfO_2, Nb_2O_5, ZrO_2, CaO, MgO, Dy_2O_3, La_2O_3, and Si_3N_4, and have a thickness within a range of about 1 nm to about 1,000 nm.

[0042] Fig. 3A illustrates a perspective view of a memory array, or 2D crossbar, 300 that includes a selector, according to an example. FIG. 3A reveals an intermediate layer 212 disposed between a first, or bottom, layer 306 of approximately parallel conductors 302 and a second, or top, layer 308 of approximately parallel conductors 304. The first layer of conductors 306 may be at a non-zero angle relative to the second layer of conductors 308 to form cross points or intersections.

[0043] Although it is clear from Fig. 3A that technically there is a three-dimensional aspect to the 2D crossbar, nevertheless, it is considered to be two-dimensional in that there is only one layer of memory cells 200a-200d. This is to be contrasted with the 3D crossbar depicted in Fig. 3B, described below, in which stacks of several layers of memory cells are provided.

[0044] According to one illustrative example, the intermediate layer 212 may be a dielectric layer, such as the insulating layer, as described in connection with Fig. 2A.

A number of the memory cells 200a-200d may be formed at the intersections, or junctions, between conductors 302 in the bottom layer 306 and conductors 304 in the top layer 308. The conductors 302, 304 may serve as the bottom and top electrodes. For example, when forming a non-volatile memory cell, such as a resistance memory cell, the conductors 302 in the bottom layer 306 may be formed from a conductive material, such as copper, aluminum, or the like, and the conductors 304 in the top layer 308 may be formed from the conductive material, which may be the same or different as the bottom layer 306.

[0045] To avoid complicating FIG. 3A, the individual layers of the memory cells 200a-200d are not shown. However, FIG. 2A, described above, provides more structural detail of the memory cells 200a-200d, with the selector 204 in series with the memory element 202. The first electrode 206 may be in electrical contact with the bottom conductors 302 and the third electrode 210 may be in electrical contact with the top conductors 304.

[0046] For purposes of illustration, only a few of the memory cells 200a-200d are shown in FIG. 3A. Each of the memory cells 200a-200d may be used to represent one or more bits of data. For example, in the simplest case, a memory cell may have two states: a low resistance state and a high resistance state. The low resistance state may represent a binary “1” and the high resistance state may represent a binary “0”, or vice versa. Binary data may be written into the nanowire memory array 300 by changing the resistance state of the matrix within the memory cells 200a-200d. The binary data can then be retrieved by sensing the resistance state of the memory cells 200a-200d. Such writing and sensing may be done using appropriate circuitry (not shown).

[0047] Fig. 3B depicts a cross-sectional view of a memory array, or 3D crossbar, also known as 3D RRAM, 350 that includes a selector, according to an example. The 3D crossbar 350 depicted in Fig. 3B may use a plurality 352 of the individual memory cells 250 depicted in Fig. 2B, each of which may include the memory element 252 integrated with the selector 254. The plurality 352 of memory elements 252, each integrated with a selector 254, may be formed in one or more stacks 354 of alternating

device layers 256 and separation layers 262, in which the device layers 256 may serve as the first electrode. At the end 256a of each device layer 256 may be provided recesses 264 in which may be formed the selector 254 and an intermediate electrode, or second electrode, 258. The memory element layer 252 may be conformally formed on the sidewalls 358 of the stacks 354 and may be in contact with the second electrodes 258. The third electrode 260 may be conformally formed on the memory element layer 252 and may be in contact with the memory element layer 252. The second electrodes 258 may be physically and electrically separated from each other.

[0048] The first electrodes 256 may each be contacted out of plane or vertically up through the center of each stack 354, much like 3D NAND Flash architecture. The device layers, or first electrodes, 256 may form bit lines, while the third electrode 260 may form source lines or vice versa.

[0049] Each stack 354 may be supported on a metallization layer 360, in turn supported on a CMOS (Complementary Metal-Oxide-Semiconductor) layer 362. The metallization layer 360 may provide electrical connections between resistive memory cells 250 and the CMOS layer 362. The CMOS layer 362 may provide processing associated with CMOS circuitry, using the resistive switching memory (e.g., memristors) as a memory medium into which information can be written and out of which information can be read.

[0050] In operation of the 3D crossbar 350, a selected memory element 252 can be individually accessed for writing or reading by applying an appropriate voltage that is higher than the threshold voltage of the selector 254 between the first electrode 256 and the third electrode 260 in contact with the selected device while the mid-point voltage may be applied all the rest of the first electrodes and the third electrodes in the array 352. Only the selector 254 in the selected device may be turned on because all the second electrodes 258 may be separated from other second electrodes. Since all the first electrodes 256 and the third electrodes 260 may be shared by a plurality of memory elements 252, if the second electrode 258 of the selected cell were connected to other second electrodes, any other cells sharing the connection would be accessed

together. It would then make it difficult to individually access a cell independently, which is why the second electrodes 258 may be isolated from each other.

[0051] As with the 2D crossbar 300, each of the devices 250 in the 3D crossbar 350 may be used to represent one or more bits of data. Also as with the 2D crossbar 300, in the simplest case, a memory device may have two states: a low resistance state and a high resistance state. Binary data may be written into the 3D crossbar 350 by changing the resistance state of the matrix within the memory devices 250. The binary data can then be retrieved by sensing the resistance state of the memory devices 250. Such writing and sensing may be done using appropriate circuitry (not shown).

[0052] By adding the amorphous stabilizing component to the selector 204, 258 as described above, namely, combining any of Si, Hf, and W with VO_x or NbO_x or a mixture thereof, the leakage current of the selectors 204, 258 can be reduced and the forming step eliminated, to thereby avoid the degradation that may accompany the forming step. The reduction of leakage current may have a substantial impact in a number of areas. The power consumption of the memory device can be reduced by reducing or eliminating the leakage current, which can be a major portion of the cell operation current. The reduced requirement for the current drivability due to the substantial reduction in row/column current in an array may make it possible to use smaller driving transistors, which is the main portion of the underlying CMOS circuit footprint that limits the density of the memory chip. The direct impact of the leakage current reduction may be the memory density increase.

[0053] By eliminating the forming step, the maximum voltage that the driving circuit has to handle may be reduced to the normal operating voltage. The reduced maximum operating voltage may enable the use of smaller transistors for the circuit, which may increase the memory density and lower the power consumption.

[0054] The amorphous stabilizing component may impede the atomic drift in the layer, which otherwise may lead to degradation of the device, and may extend the lifetime of the device.

[0055] A method for manufacturing the stable threshold switch 200, 250 may be provided. The stable threshold switch 200, 250 may include the memory element 202, 252 and the selector 204, 254, as described above. One electrode 210, 260 may contact the resistive memory 202, 252, an other electrode 206, 256 may contact the selector 204, 254, and an intermediate electrode 208, 258 may be positioned between the memory element 202, 252 and the selector 204, 254. The method may include forming in either order the memory element 202, 252 and the selector 204, 254. The selector 204, 254 may be formed in an amorphous state and may have a composition given by $(V, Nb)_{1-x}(Si, Hf, W)_xO_y$, where $0 < x < 1$ and y is within a range of 1.5 to 3.

[0056] In an example, the selector 204, 254 may be deposited as a film by sputtering a (V, Nb)-(Si, Hf, W) alloy target with an oxygen-containing gas selected from the group consisting of oxygen and water vapor.

[0057] In another example, the selector 204, 254 may be deposited as a film by sputtering a $(V, Nb)O_{Z1}$-$(Si, Hf, W)O_{Z2}$ alloy target with or without oxygen, where z1 is within a range of 2 to 2.5 and z2 is within a range of 2 to 3.

[0058] In yet another example, the selector 204, 254 may be deposited as a film by Atomic Layer Deposition. Such a method may include:

[0059] introducing a (V, Nb)-containing volatile precursor to a surface with O- or OH- terminations;

[0060] exposing the surface to an oxygen-containing gas so that oxygen in the oxygen-containing gas can react with the (V, Nb) precursor to form $(V, Nb)O_z$, where z is within a range of 2 to 2.5;

[0061] introducing a (Si, Hf, W)-containing volatile precursor to the surface;

[0062] exposing the surface to an oxygen-containing gas so that oxygen in the oxygen-containing gas can react with the (Si, Hf, W) precursor to form $(Si, Hf, W)O_z$, where z is within a range of 1.5 to 3**;** and

[0063] repeating the foregoing steps until the film having a desired thickness and composition is obtained.

[0064] Examples of the Nb-containing volatile precursor include $Nb(N(CH_3)_2)_5$ and $Nb(OCH_2CH_3)$. Examples of the Si-containing volatile precursor include

$SiH(N(CH_3)_2)$, $Si(OC_2H_5)_4$, $Si((CH_2)_3NH_2)(OC_2H_5)$, $SiCl_4$, $Si(OH)(OC(CH_3)_3)_3$, and $Si(OH)(OC(CH_3)_2(C_2H_5))_3$.

[0065] Reference throughout the specification to “one example”, “another example”, “an example”, and so forth, means that a particular element (e.g., feature, structure, and/or characteristic) described in connection with the example is included in at least one example described herein, and may or may not be present in other examples. In addition, it is to be understood that the described elements for any example may be combined in any suitable manner in the various examples unless the context clearly dictates otherwise.

[0066] It is to be understood that the ranges provided herein include the stated range and any value or sub-range within the stated range. For example, a range from about 50 to about 100 should be interpreted to include not only the explicitly recited limits of about 50 to about 100, but also to include individual values, such as 75, 90, etc., and sub-ranges, such as from about 65 to about 85, etc. Furthermore, when “about” is utilized to describe a value, this is meant to encompass minor variations (up to ±10%) from the stated value.

[0067] In describing and claiming the examples disclosed herein, the singular forms “a”, “an”, and “the” include plural referents unless the context clearly dictates otherwise.

[0068] While several examples have been described in detail, it is to be understood that the disclosed examples may be modified. Therefore, the foregoing description is to be considered non-limiting.

What is claimed is:

1. A stable threshold switching material for selectors employed in resistive memories, the material being amorphous and having a composition given by $(V, Nb)_{1-x-}$ $(Si, Hf, W)_xO_y$, where $0 < x < 1$ and y is within a range of 1.5 to 3.

2. The stable threshold switching material of claim 1 wherein the material comprises $Nb_{X-1}Si_xO_y$ alloy, where x is within a range of 0.01 to 0.9 and y is within a range of 2 to 2.5 .

3. The stable threshold switching material of claim 1 wherein the selector is combined in series with a memory element to form a memory cell.

4. The stable threshold switching material of claim 3 wherein the memory element is a resistive memory element.

5. The stable threshold switching material of claim 3 wherein the memory element comprises a material selected from the group consisting of tantalum oxide, titanium oxide, yttrium oxide, hafnium oxide, niobium oxide, zirconium oxide, aluminum oxide, calcium oxide, magnesium oxide, dysprosium oxide, lanthanum oxide, silicon dioxide, or other like oxides aluminum nitride, gallium nitride, tantalum nitride, and silicon nitride and combinations thereof.

6. The stable threshold switching material of claim 3 wherein the memory cell has an electrode contacting the memory element, an other electrode contacting the selector, and an intermediate electrode contacting both the memory element and the selector.

7. The stable threshold switching material of claim 6 wherein each electrode is independently selected from the group consisting of TiN, W, WN_2, Ta, TaN, Nb, NbN, Al, Cu, Ti, Pt, Ir, Ru, IrO_2, RuO_2, Pd, Ni, Ag, Au, Mo, and Co.

8. A method for manufacturing a stable threshold switch comprising a memory element and a selector, one electrode contacting the resistive memory, an other electrode contacting the selector, and an intermediate electrode between the memory element and the selector, the method including forming in either order the memory element and the selector, wherein the selector is formed in an amorphous state and has a composition given by $(V, Nb)_{1-x}(Si, Hf, W)_xO_y$, where $0 < x < 1$ and y is within a range of 1.5 to 3.

9. The method of claim 8 wherein the selector is deposited as a film by sputtering a (V, Nb)-(Si, Hf, W) alloy target with an oxygen-containing gas selected from the group consisting of oxygen and water vapor.

10. The method of claim 8 wherein the selector is deposited as a film by sputtering a $(V, Nb)O_{Z1}$-$(Si, Hf, W)O_{Z2}$ alloy target with or without oxygen, where z1 is within a range of 2 to 2.5 and z2 is within a range of 2 to 3.

11. The method of claim 8 wherein the selector is deposited as a film by Atomic Layer Deposition comprising:

introducing a (V, Nb)-containing volatile precursor to a surface with O- or OH-terminations;

exposing the surface to an oxygen-containing gas so that oxygen in the oxygen-containing gas can react with the (V, Nb) precursor to form $(V, Nb)O_z$, where z is within a range of 2 to 2.5;

introducing a (Si, Hf, W)-containing volatile precursor to the surface;

exposing the surface to an oxygen-containing gas so that oxygen in the oxygen-containing gas can react with the (Si, Hf, W) precursor to form $(Si, Hf, W)O_z$, where z is within a range of 1.5 to 3**;** and

repeating the foregoing steps until the film having a desired thickness and composition is obtained.

12. The method of claim 11 wherein the Nb-containing volatile precursor is selected from the group consisting of $Nb(N(CH_3)_2)_5$ and $Nb(OCH_2CH_3)$ and wherein the Si-containing volatile precursor is selected from the group consisting of $SiH(N(CH_3)_2)$, $Si(OC_2H_5)_4$, $Si((CH_2)_3NH_2)(OC_2H_5)$, $SiCl_4$, $Si(OH)(OC(CH_3)_3)_3$, and $Si(OH)(OC(CH_3)_2(C_2H_5))_3$.

13. An array of stable threshold switches comprising a plurality of memory cells, each memory cell comprising a memory element and a selector, wherein each selector is amorphous and has a composition given by $(V, Nb)_{1-x}(Si, Hf, W)_xO_y$, where $0 < x < 1$ and y is within a range of 1.5 to 3.

14. The array of claim 13 in which each memory cell is at a cross point in a 2D crossbar array.

15. The array of claim 13 in which each memory cell is incorporated in a stack of memory cells in a 3D crossbar array.

STABLE THRESHOLD SWITCHING MATERIALS FOR SELECTORS OF RESISTIVE MEMORIES

ABSTRACT

A stable threshold switching material for selectors employed in resistive memories is provided. The material is amorphous and has a composition given by $(V, Nb)_{1-x}(Si, Hf, W)_xO_y$, where $0 < x < 1$ and y is within a range of 1.5 to 3.

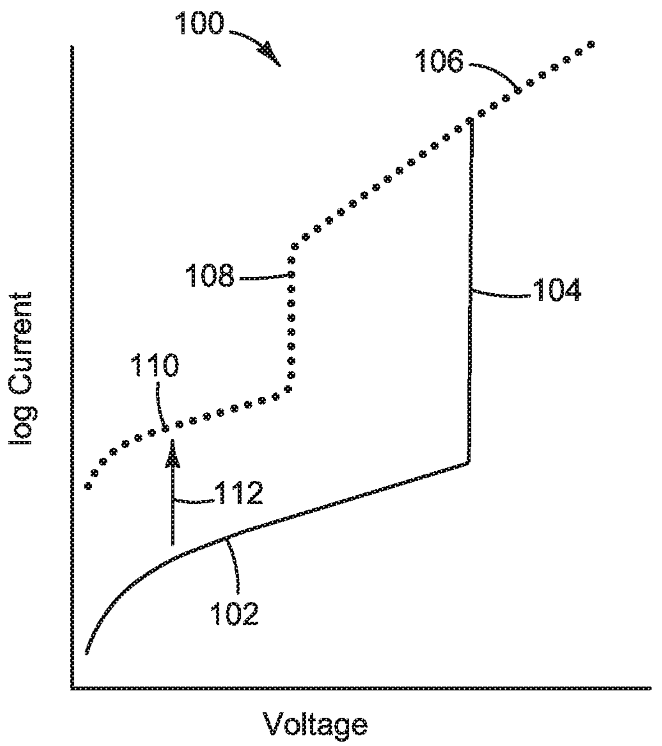

FIG. 1A

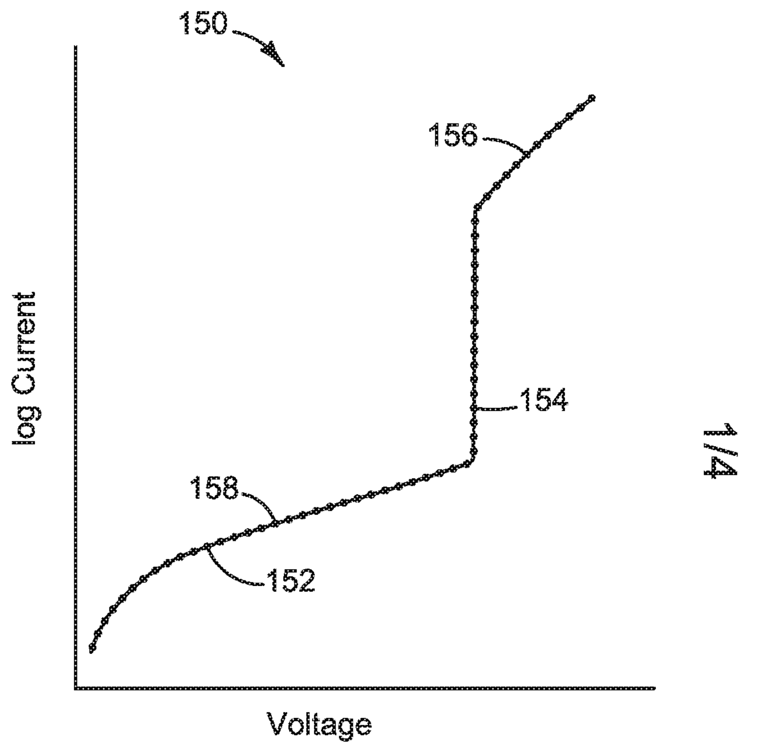

FIG. 1B

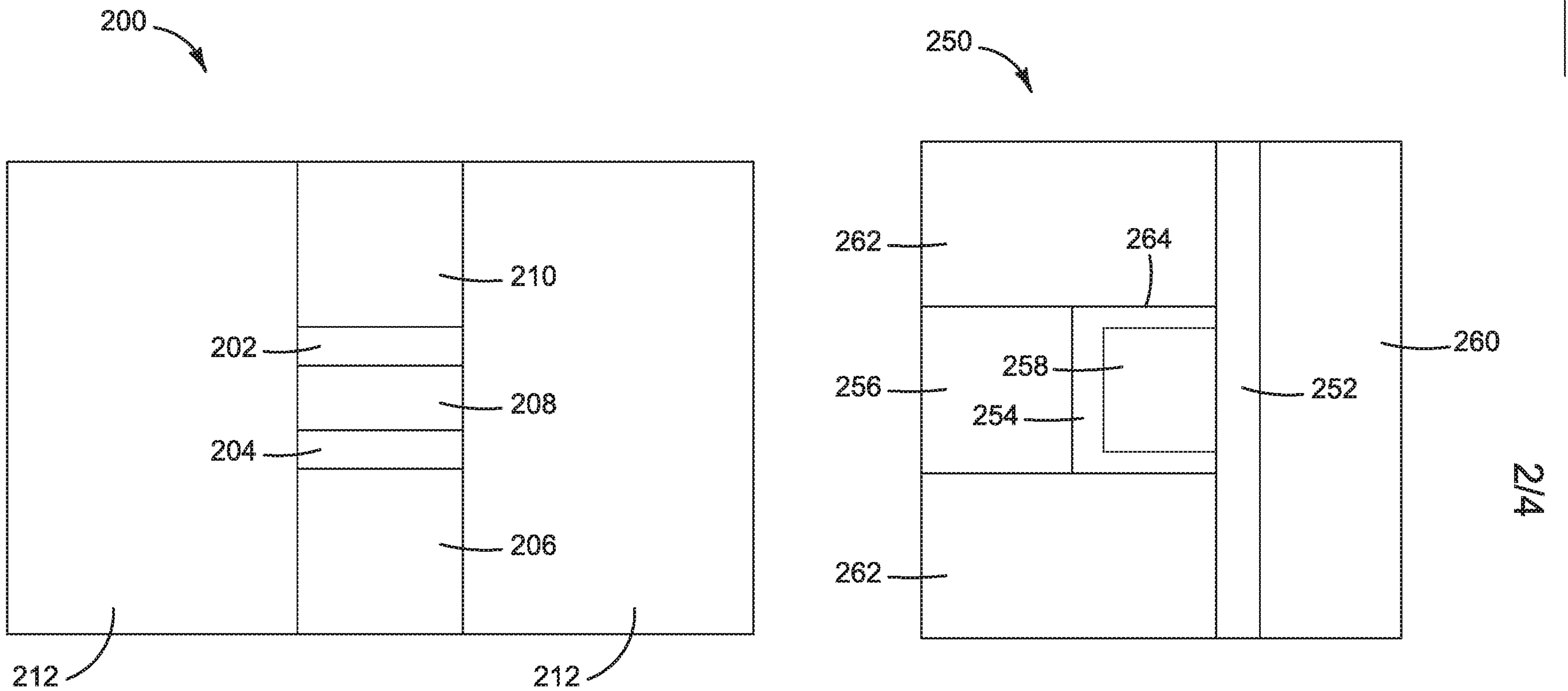

FIG. 2A

FIG. 2B

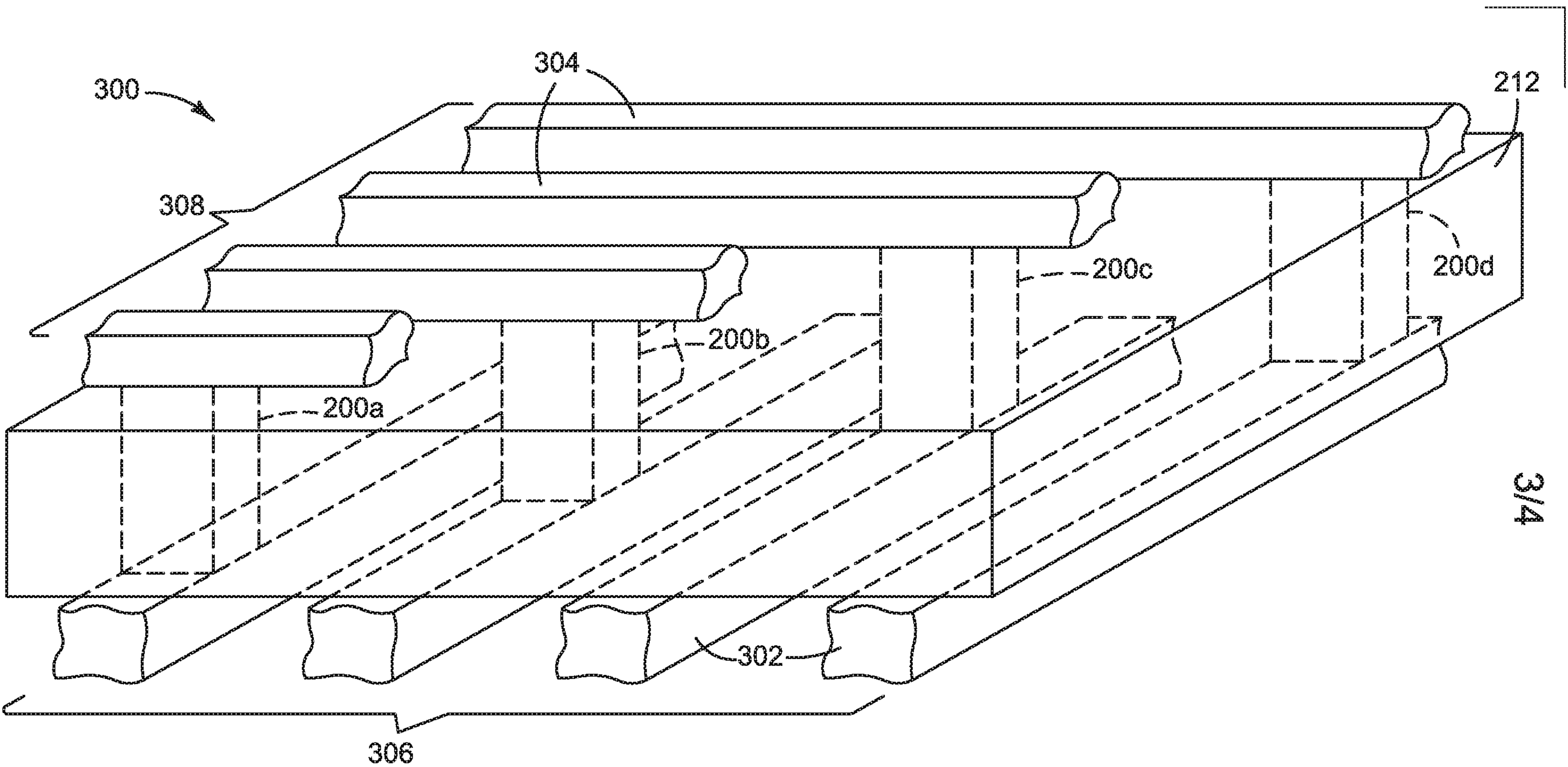

FIG. 3A

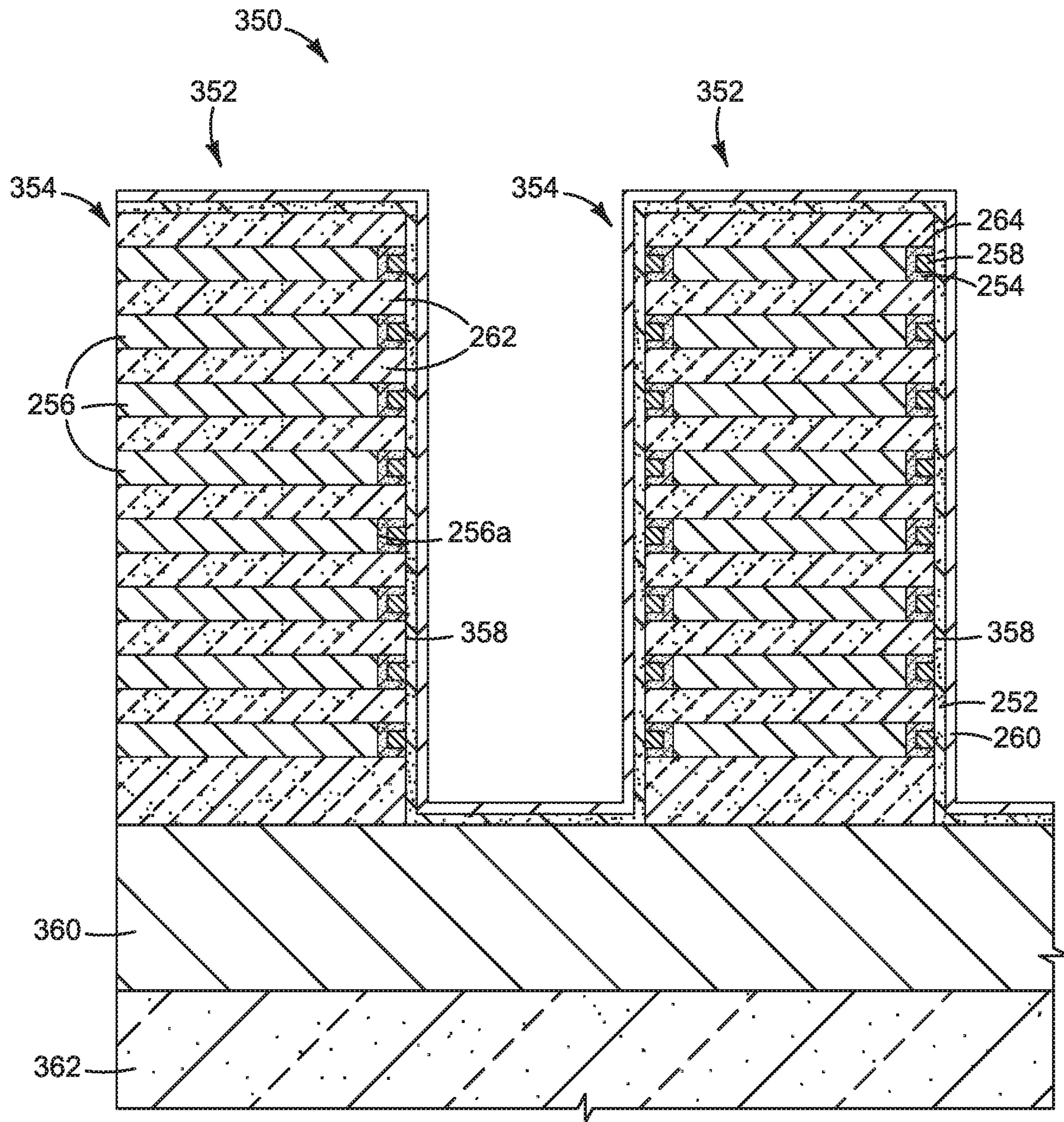

FIG. 3B