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<th>International application number:</th>
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<tr>
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<td>15 July 2015 (15.07.2015)</td>
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**Remark:** Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a),(b) or (b-bis)
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July 28, 2015

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APPLICATION NUMBER: 14/534,195
FILING DATE: November 06, 2014

THE COUNTRY CODE AND NUMBER OF YOUR PRIORITY APPLICATION, TO BE USED FOR FILING ABROAD UNDER THE PARIS CONVENTION, IS US14/534,195

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Under Secretary of Commerce
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and Director of the United States Patent and Trademark Office
**APPLICATION ELEMENTS**

1. Fee Transmittal Form (PTO/SB/17 or equivalent)
2. Applicant asserts small entity status. See 37 CFR 1.27
3. Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. Specification (Total Pages 14)
   - Such the claims and abstract must start on a new page.
   - (See MPEP § 608.01(a) for information on the preferred arrangement)

5. Drawing(s) (35 U.S.C. 113) (Total Sheets 6)
6. Inventor's Oath or Declaration (Total Pages)
   - Including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(a)(1)
   - Newly executed (original or copy)
   - A copy from a prior application (37 CFR 1.63(d))
7. Application Data Sheet *See note below.
   - See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. CD-ROM or CD-R in duplicate, large table, or Computer Program (Appendix)
   - Landscape Table on CD
9. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. –c. are required)
   - a. Computer Readable Form (CRF)
   - b. Specification Sequence Listing on:
     - i. CD-ROM or CD-R (2 copies); or
     - ii. Paper
   - c. Statements verifying identity of above copies

*Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 must be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.56(b).

**19. CORRESPONDENCE ADDRESS**

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**Signature**

/DANIEL SCHATZ/

**Date**

2014-11-06

**Registration No. (Attorney/Agent)**

59537

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DUAL SIDED CIRCUIT FOR SURFACE MOUNTING

TECHNICAL FIELD

The present invention relates to an integrated circuit for surface mounting in a circuit, the circuit having a reduced footprint with circuit elements on two sides of a substrate.

BACKGROUND

Ever since the first integrated circuits it has been desirable to reduce their size so that they may include more complex circuitry without taking up more space. Reduced size integrated circuits generally use less power, cost less and can provide faster performance. Additionally, reduced sized integrated circuits require smaller encasements and can fit more easily into other devices, for example to add GPS functionality to a smartphone or a wristwatch.

An integrated circuit may include one or more main chips and have smaller chips and/or additional elements serving as an electrical interface for the main chips. The footprint of the integrated circuit may be reduced by stacking up multiple layers, for example the main chip on one layer and the rest of the elements on another layer. This introduces the problem of communicating electrical signals between the layers especially if they are on separate substrates (e.g. printed circuit boards), thus requiring wiring between the layers.

In some methods circuit elements may be attached to the bottom side of a substrate inside the integrated circuit. Such an attachment would then require an additional substrate below it with appropriate wiring and supports if the integrated circuit is to be surface mounted onto external circuit boards.
SUMMARY

An aspect of an embodiment of the disclosure relates to a system and method of forming an integrated circuit. The integrated circuit is produced from a first substrate layers. The substrate layer has three pieces: a center piece and side pieces on two opposite sides of the center piece.

The center piece is designed for assembling circuit elements on the top and on the bottom. The side pieces include via connectors that electrically connect between the top of the substrate, the bottom of the substrate and may connect also to circuit elements on the center piece. The connection between the circuit elements and the via connectors may be done by printing on the substrate, electrical elements or internally in the design of the substrate layer.

Two substrate pieces about the size of the side pieces are coupled to the bottom of the side pieces to support the first substrate layer and form a void under the center piece to leave room for the circuit elements attached to the bottom of the first substrate layer. The supports include via connectors that provide an electrical connection between the bottom of the support and the top. The via connectors of the supports connect to the via connectors of the side pieces and form electrical contact between the bottom of the supports and the bottom of the side pieces, which then connect to the electrical elements.

In an exemplary embodiment of the disclosure, the substrate layers are formed from wafers having multiple dies. The first substrate layer is formed from three consecutive dies. Optionally, the center die may have a different design than the side dies to enable it to accommodate circuit elements. In an exemplary embodiment of the disclosure, the side dies have an array of via connectors and may be cut so that only some of the columns of the array will remain as part of the integrated circuit.

There is thus provided according to an exemplary embodiment of the disclosure, a method of forming an integrated circuit, comprising:

Providing a first substrate layer having a center piece and two side pieces on opposite sides of the center piece;
Assembling one or more circuit elements on a top side and a bottom side of the center piece of the first substrate layer;

Preparing two support pieces from a substrate, matching the size of the side pieces;

Coupling the support pieces to the bottom of the first substrate layer under the side pieces to form a second substrate layer with a void in the center under the center piece of the first substrate layer; and

Wherein the side pieces and support pieces include via connectors electrically connecting between a bottom side of the second substrate layer and the circuit elements.

In an exemplary embodiment of the disclosure, the method further comprises cutting off part of the side pieces and the support pieces along a pre-selected cut line to reduce the size of a footprint of the integrated circuit. Optionally, the support pieces are each formed from a single die of a cut up wafer. In an exemplary embodiment of the disclosure, the die of the support pieces comprise an array of via connectors that electrically connect between the top of the support piece to the bottom of the support piece. Optionally, the first substrate layer is formed from a wafer having multiple die. In an exemplary embodiment of the disclosure, the wafer includes two types of die forming a checkerboard pattern. Optionally, the integrated circuit is formed by assembling the circuit elements on one type of die and assembling the support pieces on the second type of die. In an exemplary embodiment of the disclosure, the wafer is cut up to form the integrated circuit; wherein the first substrate layer of each integrated circuit includes one die with circuit elements assembled thereon serving as the center piece and two side pieces extending from opposite sides of the center piece, each side piece having support pieces attached thereon.

There is further provided according to an exemplary embodiment of the disclosure, an integrated circuit, comprising:

A first substrate layer having a center piece and two side pieces on opposite sides of the center piece;
Circuit elements assembled on a top side and on a bottom side of the center piece of a first substrate layer;

Two support pieces made from a substrate matching the size of the side pieces;

Wherein the support pieces are coupled to the bottom of the first substrate layer under the side pieces to form a second substrate layer with a void in the center under the center piece of the first substrate layer; and

Wherein the side pieces and support pieces include via connectors electrically connecting between a bottom side of the second substrate layer and the circuit elements.

In an exemplary embodiment of the disclosure, part of the side pieces and the support pieces are cut off along a pre-selected cut line to reduce the size of a footprint of the integrated circuit. Optionally, the support pieces are each formed from a single die of a cut up wafer. In an exemplary embodiment of the disclosure, the die of the support pieces comprise an array of via connectors, that electrically connect between the top of the support piece to the bottom of the support piece. Optionally, the first substrate layer is formed from a wafer having multiple die. In an exemplary embodiment of the disclosure, the wafer includes two types of die forming a checkerboard pattern. In an exemplary embodiment of the disclosure, the integrated circuit is formed by assembling the circuit elements on one type of die and assembling the support pieces on the second type of die. Optionally, the wafer is cut up to form the integrated circuit; wherein the first substrate layer of each integrated circuit includes one die with circuit elements assembled thereon serving as the center piece and two side pieces extending from opposite sides of the center piece, each side piece having support pieces attached thereon.
BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure will be understood and better appreciated from the following detailed description taken in conjunction with the drawings. Identical structures, elements or parts, which appear in more than one figure, are generally labeled with the same or similar number in all the figures in which they appear, wherein:

Fig. 1A is a schematic illustration of circuit on a first substrate layer with supports for assembling a dual sided surface mountable integrated circuit, according to an exemplary embodiment of the disclosure;

Fig. 1B is a schematic illustration of a circuit on a first substrate layer with supports coupled together to form a dual sided surface mountable integrated circuit, according to an exemplary embodiment of the disclosure;

Fig. 1C is a schematic illustration of a top view of a dual sided surface mountable integrated circuit, according to an exemplary embodiment of the disclosure;

Fig. 1D is a schematic illustration of a bottom view of a dual sided surface mountable integrated circuit, according to an exemplary embodiment of the disclosure;

Fig. 2A is a schematic illustration of a first type of wafer of substrate dies for forming a dual sided surface mountable integrated circuit, according to an exemplary embodiment of the disclosure;

Figs. 2B is a schematic illustrations of a second type of wafer of substrate dies for forming a dual sided surface mountable integrated circuit, according to an exemplary embodiment of the disclosure;

Fig. 3 is a flow diagram of a method of forming a dual sided surface mountable integrated circuit, according to an exemplary embodiment of the disclosure; and

Fig. 4 is a schematic illustration of dual sided surface mountable integrated circuit deployed in a circuit, according to an exemplary embodiment of the disclosure.

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DETAILED DESCRIPTION

Fig. 1A is a schematic illustration of circuit on a first substrate layer 110 with supports (122 and 126) for assembling a dual sided surface mountable integrated circuit 100 and Fig. 1B is a schematic illustration of a circuit on first substrate layer 110 coupled together with the supports (122, 126) to form dual sided surface mountable integrated circuit 100, according to an exemplary embodiment of the disclosure. In an exemplary embodiment of the disclosure, first substrate layer 110 includes three pieces a first side piece 112, a second side piece 116 and a center piece 114.

In an exemplary embodiment of the disclosure, circuit elements 150 are assembled on center piece 114 of first substrate layer 110. Optionally, one or more circuit elements 160 are assembled under center piece 114 on the bottom of first substrate layer 110. In an exemplary embodiment of the disclosure, supports 122 and 126 are placed under first side piece 112 and second side piece 116 respectively to form a second substrate layer 120 for integrated circuit 100 with a void 125 under center piece 114. Optionally, first side piece 112 and second side piece 116 include via connectors 170 that provide an electrical connection from the top side of the first substrate layer 110 to the bottom side of the first substrate layer 110. Likewise supports 122 and 126 include similar via connectors 170 for second layer 120 matching the position of via connectors 170 on the first substrate layer 110 to form an electrical connection from the electrical elements on the first substrate layer 110 to the bottom of second layer 120. In an exemplary embodiment of the disclosure, the via connectors 170 are electrically connected to the circuit elements (150, 160) mounted on center piece 114, thus forming contact between the bottom of second layer 120 and the circuit on first substrate layer 110. In some embodiments of the disclosure, the via connectors 170 on the first substrate layer 110 are not visible on the top of the first substrate layer 110.

In an exemplary embodiment of the disclosure, the substrate layers (110, 120) are coupled together using adhesives, using pressure, using solder or other methods known in the art such that the via connectors 170 of the two
substrate layers are electrically connected. Accordingly, integrated circuit 100 may be surface mounted on an external electrical circuit with electrical contact between the external electrical circuit and the elements of integrated circuit 100 through the via connectors 170 of the second substrate layer 120.

In an exemplary embodiment of the disclosure, the first substrate layer 110 may comprise a single layer, dual layer or multilayer substrate to accommodate any type of electrical circuit and circuit element. Optionally, the thickness of the substrate layers may be identical or may vary depending on the requirements of the integrated circuit 100. For example the thickness of second substrate layer 120 may be selected to exactly accommodate circuit elements 160 in void 125. Optionally, the thickness may be the same as the tallest element of circuit elements 160 or may be larger leaving a space between circuit elements 160 and a substrate on which integrated circuit 100 is surface mounted.

In an exemplary embodiment of the disclosure, the first side piece 112 and second side piece 116 of first substrate layer 110 together with the supports 122, 126 are cut at a cut line 140 leaving a small portion of the side pieces with the via connectors 170 on each side in contact with the center piece 114.

Fig. 1C is a schematic illustration of a top view of a dual layer surface mountable integrated circuit 100 and Fig. 1D is a schematic illustration of a bottom view of a dual layer surface mountable integrated circuit 100, according to an exemplary embodiment of the disclosure. Elements 150 can be seen in Fig. 1C on top of substrate 110 and element/elements 160 can be seen in Fig. 1D on the bottom of integrated circuit 100.

In an exemplary embodiment of the disclosure, circuit element 160 may be a GPS chip such as GSD4e-9333 manufactured by CSR plc from Cambridge England and circuit elements 150 are used to interface the GPS chip. Instead of manufacturing an integrated circuit with a large footprint (e.g. 10mm X 10mm) to accommodate the GPS chip and the interface elements, integrated circuit 100 can be used to form an integrated circuit 100 with a footprint of less than 5mm X 5 mm (e.g. 4mm X 4mm) providing the same functionality.
In an exemplary embodiment of the disclosure, substrate layers (110, 120) are formed from wafers with multiple dies. Fig. 2A is a schematic illustration of a first type of wafer 200 of substrate dies for forming a multi-layer integrated circuit and Figs. 2B is a schematic illustration of a second type of wafer 250 of substrate dies for forming a multi-layer integrated circuit, according to an exemplary embodiment of the disclosure. In an exemplary embodiment of the disclosure, wafer 200 includes two types of dies (210, 220) in a checkerboard form with or without a space between each row of the wafer 200. The first type 210 serves as first side piece 112 and second side piece 116 with via connectors 170. The second type 220 serves as center piece 114 for installing elements 150 and 160.

In an exemplary embodiment of the disclosure, wafer 250 includes only one type of die 230 with via connecters 170. Optionally, die 230 are identical to die 210. Alternatively, die 230 may have via connecters 170 from the bottom to the top whereas die 210 may be manufactured having an electrical connection connecting via connecters 170 to center piece 114, either internally or on the bottom or top.

In an exemplary embodiment of the disclosure, wafer 250 is cut up entirely into die 230. Unit 255 illustrates an enlarged view of 3 die 230 with lines 240 marking the cutting position for separating the die 230.

In an exemplary embodiment of the disclosure, circuit elements 150 and 160 are assembled on die 220 of wafer 200. Likewise die 230 are coupled to die 210 on the same side as element/elements 160. After assembling elements 150, 160 and die 230 on wafer 200, wafer 200 is cut up along cut lines 140 leaving via connecters 170 from die 230 as part of integrated circuit 100.

Fig. 3 is a flow diagram of a method 300 of forming a dual sided surface mountable integrated circuit 100, according to an exemplary embodiment of the disclosure.

In an exemplary embodiment of the disclosure, a first substrate layer 110 is provided (310). The first substrate layer 110 has:
(I) a center piece 114 for installing circuit elements (150, 160);
(II) a first side piece 112 on one side of the center piece 114; and
(III) a second side piece 116 on an opposite side of the center piece 114.

In an exemplary embodiment of the disclosure, the side pieces have via
connectors 170 connecting between the top side and the bottom side of each
substrate. Optionally, one or more circuit elements 150 are assembled (320) on
the top of the center piece 114 of the first substrate layer 110 and/or one or more
circuit elements 160 are assembled (320) on the bottom of the center piece 114 of
the first substrate layer 110. In an exemplary embodiment of the disclosure, the
via connectors 170 are electrically connected to the circuit elements (150, 160) to
enable mounting the integrated circuit 100 on an external circuit.

In an exemplary embodiment of the disclosure, two support pieces
(122, 126) are prepared (330) from a substrate to match the first side piece 112
and the second side piece 116 respectively. Optionally, the support pieces (122,
126) are coupled (340) to the first substrate layer 110 forming an integrated
circuit 100 having a second substrate layer 120 with a void 125 to accommodate
the circuit elements (160) installed under the center piece 114 of the first substrate
layer 110.

In an exemplary embodiment of the disclosure, the substrate layers
(110, 120) are cut (350) on cut line 140 to reduce the size of the footprint of the
integrated circuit. Optionally, after cutting the substrate layers (110, 120) the via
connectors 170 remain a part of the integrated circuit 100 and the rest of the side
pieces (112, 116) and supports (122, 126) are removed leaving a fraction of the
original pieces, for example 1/3, 1/4, 1/5 or even 1/10.

Fig. 4 is a schematic illustration of dual sided surface mountable
integrated circuit 100 deployed in an external circuit 400, according to an
exemplary embodiment of the disclosure. As explained above first side piece 112,
second side piece 116 and supports (122, 126) were cut along cut lines 140 to
form the final form of integrated circuit 100. Optionally, the final form is then surface mounted onto external circuit 400.

It should be appreciated that the above described methods and apparatus may be varied in many ways, including omitting or adding steps, changing the order of steps and the type of devices used. It should be appreciated that different features may be combined in different ways. In particular, not all the features shown above in a particular embodiment are necessary in every embodiment of the disclosure. Further combinations of the above features are also considered to be within the scope of some embodiments of the disclosure. It will also be appreciated by persons skilled in the art that the present disclosure is not limited to what has been particularly shown and described hereinabove.
FIG. 1A

FIG. 1B
PROVIDE A FIRST SUBSTRATE LAYER HAVING A CENTER PIECE, A FIRST SIDE PIECE AND A SECOND SIDE PIECE

ASSEMBLE CIRCUIT ELEMENTS ON BOTH SIDES OF THE CENTER PIECE OF THE FIRST SUBSTRATE LAYER

PREPARE TWO SUPPORT PIECES FROM A SUBSTRATE TO MATCH THE FIRST SIDE PIECE AND SECOND SIDE PIECE

COUPLE THE SUPPORT PIECES TO THE SIDE PIECES OF THE FIRST SUBSTRATE LAYER. THE SUPPORT PIECES SERVING AS A SECOND SUBSTRATE LAYER WITH A VOID IN THE CENTER TO ACCOMMODATE THE CIRCUIT ELEMENTS UNDER THE CENTER PIECE OF THE FIRST SUBSTRATE LAYER

CUT OFF PART OF THE SIDE PIECES FROM THE FIRST SUBSTRATE LAYER AND THE SECOND SUBSTRATE LAYER

FIG. 3
CLAIMS

I/We claim:

1. A method of forming an integrated circuit, comprising:
   providing a first substrate layer having a center piece and two side pieces on opposite sides of the center piece;
   assembling one or more circuit elements on a top side and a bottom side of the center piece of the first substrate layer;
   preparing two support pieces from a substrate, matching the size of the side pieces;
   coupling the support pieces to the bottom of the first substrate layer under the side pieces to form a second substrate layer with a void in the center under the center piece of the first substrate layer; and
   wherein the side pieces and support pieces include via connectors electrically connecting between a bottom side of the second substrate layer and the circuit elements.

2. A method according to claim 1, further comprising cutting off part of the side pieces and the support pieces along a pre-selected cut line to reduce the size of a footprint of the integrated circuit.

3. A method according to claim 1, wherein the support pieces are each formed from a single die of a cut up wafer.

4. A method according to claim 3, wherein the die of the support pieces comprise an array of via connectors that electrically connect between the top of the support piece to the bottom of the support piece.
5. A method according to claim 1, wherein the first substrate layer is formed from a wafer having multiple die.

6. A method according to claim 5, wherein the wafer includes two types of die forming a checkerboard pattern.

7. A method according to claim 6, wherein the integrated circuit is formed by assembling the circuit elements on one type of die and assembling the support pieces on the second type of die.

8. A method according to claim 7, wherein the wafer is cut up to form the integrated circuit; wherein the first substrate layer of each integrated circuit includes one die with circuit elements assembled thereon serving as the center piece and two side pieces extending from opposite sides of the center piece, each side piece having support pieces attached thereon.

9. An integrated circuit, comprising:
   a first substrate layer having a center piece and two side pieces on opposite sides of the center piece;
   circuit elements assembled on a top side and on a bottom side of the center piece of a first substrate layer;
   two support pieces made from a substrate matching the size of the side pieces;
   wherein the support pieces are coupled to the bottom of the first substrate layer under the side pieces to form a second substrate layer with a void in the center under the center piece of the first substrate layer; and
   wherein the side pieces and support pieces include via connectors electrically connecting between a bottom side of the second substrate layer and the circuit elements.
10. An integrated circuit according to claim 9, wherein part of the side pieces and the support pieces are cut off along a pre-selected cut line to reduce the size of a footprint of the integrated circuit.

11. An integrated circuit according to claim 9, wherein the support pieces are each formed from a single die of a cut up wafer.

12. An integrated circuit according to claim 11, wherein the die of the support pieces comprise an array of via connectors that electrically connect between the top of the support piece to the bottom of the support piece.

13. An integrated circuit according to claim 9, wherein the first substrate layer is formed from a wafer having multiple die.

14. An integrated circuit according to claim 13, wherein the wafer includes two types of die forming a checkerboard pattern.

15. An integrated circuit according to claim 14, wherein the integrated circuit is formed by assembling the circuit elements on one type of die and assembling the support pieces on the second type of die.

16. An integrated circuit according to claim 15, wherein the wafer is cut up to form the integrated circuit; wherein the first substrate layer of each integrated circuit includes one die with circuit elements assembled thereon serving as the center piece and two side pieces extending from opposite sides of the center piece, each side piece having support pieces attached thereon.
ABSTRACT

A method of forming an integrated circuit, including providing a first substrate layer having a center piece and two side pieces on opposite sides of the center piece, assembling one or more circuit elements on a top side and a bottom side of the center piece of the first substrate layer, preparing two support pieces from a substrate, matching the size of the side pieces, coupling the support pieces to the bottom of the first substrate layer under the side pieces to form a second substrate layer with a void in the center under the center piece of the first substrate layer; and wherein the side pieces and support pieces include via connectors electrically connecting between a bottom side of the second substrate layer and the circuit elements.
DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention: DUAL SIDED CIRCUIT FOR SURFACE MOUNTING

As the below named inventor, I hereby declare that:

This declaration is directed to:  
✓ The attached application, or
☐ United States application or PCT international application number ______________
filed on ______________.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Haim GOLDBERGER  
Date (Optional): Oct 5, 2014

Signature: ____________________________

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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<td>First Named inventor</td>
<td>Haim GOLDBERGER</td>
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This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.
POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

☐ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

67305

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

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Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

☐ The address associated with the above-mentioned Customer Number.

☐ The address associated with Customer Number: ____________________________

☐ Firm or Individual Name: ____________________________

Address: ____________________________

City: ____________________________
State: ____________________________
Zip: ____________________________

Country: ____________________________

Telephone: ____________________________

Email: ____________________________

I am the Applicant:

☐ Inventor or Joint Inventor
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor
☐ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

Signature: ____________________________ Date: Oct. 5, 2019

Name: ____________________________
Title and Company: ____________________________
Telephone: ____________________________

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below.

☐ Total of _______ forms are submitted.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
Application Data Sheet 37 CFR 1.76

Attorney Docket Number 5154/8.3
Application Number

Title of Invention DUAL SIDED CIRCUIT FOR SURFACE MOUNTING

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2. (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1
Legal Name
Prefix Haim
Given Name
Middle Name
Family Name GOLDBERGER
Suffix
Residence Information (Select One) ☐ US Residency ☐ Non US Residency ☐ Active US Military Service
City Mid’ln
Country of Residence IL

Mailing Address of Inventor:
Address 1 31 Nahal Snir Street
Address 2
City Mid’ln
State/Province
Postal Code 7170964 Country IL

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence Information of this application.

Customer Number 67305
Email Address mail@ip-law.co.il

Application Information:

Title of the Invention DUAL SIDED CIRCUIT FOR SURFACE MOUNTING
Attorney Docket Number 5154/8.3 Small Entity Status Claimed ☒
Application Type Nonprovisional
Subject Matter Utility
Total Number of Drawing Sheets (if any) 6 Suggested Figure for Publication (if any)
## Application Data Sheet 37 CFR 1.76

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### Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

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### Publication Information:

- [ ] Request Early Publication (Fee required at time of Request 37 CFR 1.219)

- **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

### Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

- [ ] Customer Number
- [ ] US Patent Practitioner
- [ ] Limited Recognition (37 CFR 11.9)

Customer Number: 67305

### Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78. When referring to the current application, please leave the application number blank.

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Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.

### Foreign Priority Information:

EFS Web 2.2.11
Application Data Sheet 37 CFR 1.76

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This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX), the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Additional Foreign Priority Data may be generated within this form by selecting the Add button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices
Application Data Sheet 37 CFR 1.76

Title of Invention  DUAL SIDED CIRCUIT FOR SURFACE MOUNTING

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed.

The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an assignee (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

- Assignee
- Legal Representative under 35 U.S.C. 117
- Joint Inventor
- Person to whom the inventor is obligated to assign.
- Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name: ORIGIN GPS LTD.

Mailing Address Information For Applicant:

Address 1  2 Negev Street, P.O.B 112

Address 2

City  Airport City  State/Province

Country  IL  Postal Code  7015002

Phone Number

Fax Number
# Application Data Sheet 37 CFR 1.76

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**Title of Invention:** DUAL SIDED CIRCUIT FOR SURFACE MOUNTING

**Email Address:**

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### Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

**Assignee 1**

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Assignee Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. [ ]

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### Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

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