PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

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PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/IB2012/001774	22.08.2012	

International Patent Classification (IPC) or both national classification and IPC
INV. H01L27/02

Applicant
FREESCALE SEMICONDUCTOR, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office Gitschiner Str. 103 D-10958 Berlin Tel. +49 30 25901 - 0 Fax: +49 30 25901 - 840	see form PCT/ISA/210	Morena, Enrico Telephone No. +49 30 25901-771

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/IB2012/001774

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

   ☐ on paper

   ☐ in electronic form

   b. (time)

   ☐ in the international application as filed

   ☐ together with the international application in electronic form

   ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-9, 15-19
	No:	Claims	10-14
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-19
Industrial applicability (IA)	Yes:	Claims	1-19
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following documents:

D1 EP 2 442 359 A1 (FREESCALE SEMICONDUCTOR INC [US]) 18 April 2012 (2012-04-18)

D2 US 2011/169092 A1 (IKUTA TERUHISA [JP] ET AL) 14 July 2011 (2011-07-14)

D5 US 2011/176244 A1 (GENDRON AMAURY [US] ET AL) 21 July 2011 (2011-07-21)cited in the application

2 The present application does not meet the requirements of Article 33(2) PCT because the subject-matter of claims 10-14 is not new.

2.1 Concerning the subject-matter of independent claim 10, document D1 discloses an ESD protection circuit for protecting an integrated circuit against ESD events received by the integrated circuit, the ESD protection circuit comprising:
- a first terminal (see D1, figure 3, reference "Vdd")suitable for being coupled to an I/O pad of the integrated circuit,
- a second terminal (see D1, figure 3, reference "Vss") suitable for being coupled to a most negative voltage available on the semiconductor device under normal operational condition or to a ground voltage,
- a third terminal (intrinsic feature of the device of figure 3 of D1) for being coupled to a substrate of a semiconductor device wherein the ESD protection circuit is being manufactured,
- a common terminal (see D1, figure 3, reference 313),
- a first diode (see D1, figure 3, diode between 305,308-2,311 and Nwell 307-2), an anode of the first diode being coupled to the first terminal and a cathode of the first diode being coupled to the common terminal,
- a second diode (see D1, figure 3, diode between 305,308-1,310 and Nwell), an anode of the second diode being coupled to the second terminal and a cathode of the second diode (D2) being coupled to the common terminal, and
- a third diode (see D1, figure 3, diode between P-substrate and Nwell) having a high voltage breakdown voltage, an anode of the third diode being coupled to the third terminal and a cathode of the third diode being coupled to the common terminal.

The circuit defined by claim 10 also constitutes the electrical model of the structure disclosed by document D3 (see D3, figure 5).

2.2 Dependent claims 11-14 do not contain any feature which, in combination with the features of the claims to which they refer, meet the requirements of the PCT in respect of novelty (Article 33(2) PCT)), the reasons being as follows:

a) (claim 11) 70volts is encompasses by breakdown voltages for advanced smart power technologies as such disclosed by document D1;

b) (claim 12) substrate is usually connected to ground;

c) (claim 13) Vss is usually coupled to ground;

d) (claim 14) document D1 relates to an ESD protection within an integrated circuit (see D1, abstract).

3 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1-9, 15-19 does not involve an inventive step in the sense of Article 33(3) PCT, the reasons being as follows:

3.1 Concerning the subject-matter of independent claim 1, document D1, which is considered to represent the closest prior art, discloses a semiconductor device comprising an ESD protection device for protecting an integrated circuit on the semiconductor device against ESD event received by the integrated circuit, the ESD protection device comprising

- a semiconductor substrate (see D1, figeru 3, reference 303), the semiconductor substrate having a first side, the semiconductor substrate having an N-buried region (see D1, figure 3, reference 304) extending in a lateral direction in the interior of the semiconductor substrate,
- a p-doped isolated portion of the semiconductor substrate (see D1, figure 3, reference 305)being isolated from a remaining part of the semiconductor substrate by an isolation structure, the isolation structure comprising the N-buried region (NBL, 236),
- an N-doped region (see D1, figure 3, reference "N-well") being arranged in the p-doped isolated portion and extending from the first side towards the N-buried region, the N-doped region subdividing the isolated portion in a first portion and a second portion,
- a first p-doped region (see D1, figure 3, reference 308-1) and a second p-doped region (see D1, figure 3, reference 308-2)extending from the first side into, respectively, the first portion and the second portion, the p-dopant concentration of the first p-doped region and of the second p-doped region being higher than the p-dopant concentration of the first portion and the

second portion,
- a first contact region (see D1, figure 3, reference 311) and a second contact region (see D1, figure 3, reference 310) extending from the first side, respectively, into the first p-doped region and into the second p-doped region, the first contact region and the second contact region being p-doped with a dopant concentration being higher than the p-dopant concentration of the first p-doped region and of the second p-doped region,
- a first electrical contact (see D1, figure 3, reference 323) being electrically connected to the first p-doped region only via the first contact region, the first electrical contact being configured for being connected to an I/O pad of the semiconductor device,
- a second electrical contact (see D1, figure 3, reference 320) being electrically connected to the second p-doped region via the second contact region, the second electrical contact being configured for being connected to a most negative voltage available on the semiconductor device under normal operational condition or to a ground voltage (gnd),

3.1.1 The subject-matter of claim 1 differs from the explicit disclosure of document D1 in that:

i) the second electrical contact is electrically connected to the second p-doped region only via the second contact region (emphases added);

and in that the claimed device further comprises:

ii) a third electrical contact being electrically connected to the remaining part of semiconductor substrate, the third electrical contact being configured for being connected to the ground voltage).

3.1.2 Concerning the differences at point ii), it is considered that an electrical contact to the underlying substrate is a intrinsic feature of a smart power device disclosed by document D1.

3.1.3 The technical problem to be solved by the present application can be regarded as to avoid snap-back in the protection device.

3.1.4 The solution defined by present claim 1 can not be considered to involve an inventive step, because the person skilled in the art would recognize that the snap-back can be avoided by avoiding the formation of the NPN of the SCR of document D1. Such an approach is known and it has been detailed in document D2 (see D2, figure 2, paragraph 56).

The person skilled in the art would realize that by omitting the formation of the n+ contact (see D1, figure 3, reference 312), he would easily obtain the "snap-back free" protection of document D2. He would also obtain the advantage of further reducing the are occupied by the protection element, as it is already discussed in document D1 in relation with the omission of the n+ contact in the anode region (right end side of figure 3 of document D3.

Consequently, claim 1 does not meet the requirements of the PCT in respect of inventive step (Article 33(3) PCT).

3.1.5 It seems worth to point out that the subject-matter of claim 1 is considered not to in volve an inventive step also when starting from the disclosure of document D2. The subject-matter of claim 1 differs from the ESD protection of document D2 in that the claimed device is isolated by the buried layer, whereas the device of document D2 is on an SOI substrate. Both technology are well known and commonly adopted in smart power application, so that the implementation of the structure of document D2 in a junction-isolated process is considered a mere design choice, that the person skilled in the art would take according to the circumstances, without the exercise of any inventive activity.

3.2 The same arguments equally apply to the subject-matter of corresponding method claim 15, which is also considered not to meet the requirements of the PCT in respect of inventive step (Article 33(3) PCT).

3.3 Dependent claims 2-9 and 16-19 do not contain any feature which, in combination with the features of the claims to which they refer, meet the requirements of the PCT in respect of inventive step (Article 33(3) PCT)), since they relate to known details of implementation, disclosed in documents D1-D3.

4 All claims 1-19 are considered as industrially applicable and therefore meet the criteria of Article 33(4) PCT.