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- (71) **Applicant (for all designated States except US):** VNS PORTFOLIO LLC [US/US]; 20400 Stevens Creek Blvd., Fifth Floor, Cupertino, CA 95014 (US).
- (72) **Inventor; and**
- (75) **Inventor/Applicant (for US only):** MOORE, Charles, H. [US/US]; 110 Greene Rd., Sierra City, CA 96125 (US).
- (74) **Agent:** HENNEMAN, JR., Larry, E.; Henneman & Associates, PLC, 70 N. Main St., Three Rivers, MI 49093 (US).
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(54) **Title:** METHOD AND APPARATUS FOR REDUCING LATENCY ASSOCIATED WITH EXECUTING MULTIPLE INSTRUCTION GROUPS

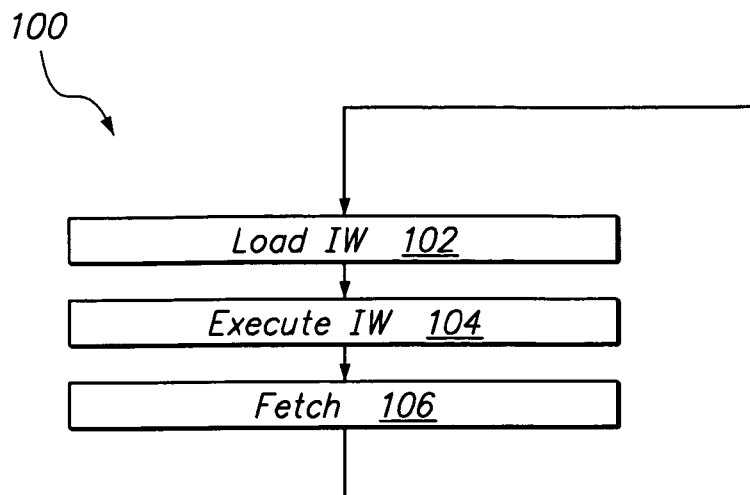


FIG. 1

(57) **Abstract:** A method and apparatus for reducing latency in computer processors. The method incorporates a special instruction set that provides an indication of whether a particular instruction is capable of being executed nearly simultaneously with a preceding instruction in the same group. In such a situation, multiple instructions may be executed at a rate faster than expected. A simple apparatus for accomplishing this method is illustrated.

WO 2010/030353 A3

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 9/30; G06F 15/00; G06F 9/00; G06F 9/40; G06F 9/45

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models
(Chinese Patents and application for patent)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: latency reduction, predict, ALU instruction

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005-0216703 A1 (DIEFFENDERFER, J. N. et al.) 29 September 2005 See the abstract, fig.2, paras.[0009]-[0010], [0018]-[0022], and [0024]-[0025]	1-22
A	US 2002-0124162 A1 (YUNG, R. et al.) 05 September 2002 See the abstract, fig.1, paras.[0010]-[0014], claim 1	1-22
A	US 2003-0046518 A1 (KARP, A. H. et al.) 06 March 2003 See the abstract, paras.[0007], [0014]-[0016], and [0020], claims 1-2	1-22
A	US 2007-0055961 A1 (CALLISTER, J. R. et al.) 08 March 2007 See the abstract, fig.7, paras.[0011] and [0049]	1-22

 Further documents are listed in the continuation of Box C. See patent family annex.

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Authorized officer

Park Ji Eun

Telephone No. 82-42-481-5696



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US 2007-0055961 A1	08.03.2007	None	