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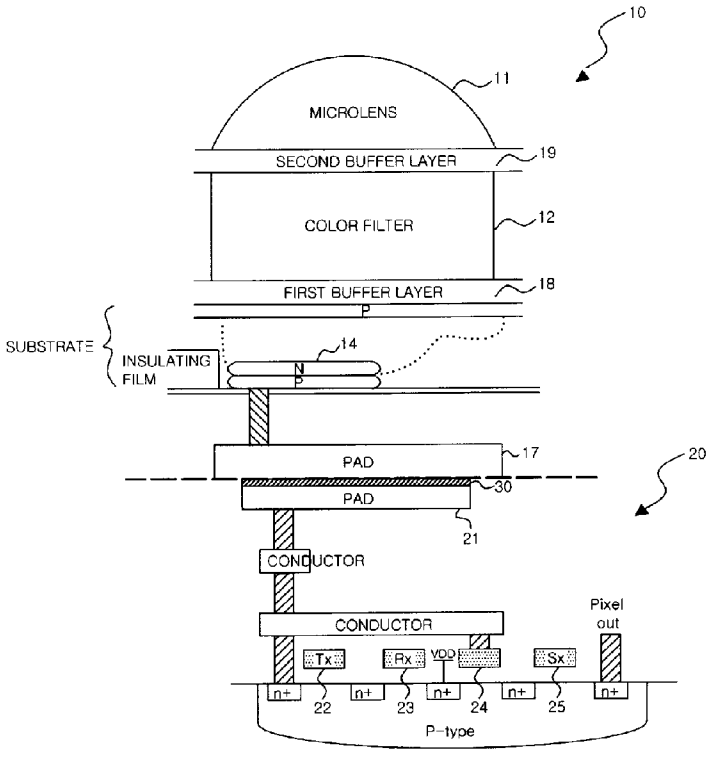
(54) **Title:** SEPARATION TYPE UNIT PIXEL OF 3-DIMENSIONAL IMAGE SENSOR AND MANUFACTURING METHOD THEREOF



(57) **Abstract:** A separation type unit pixel of an image sensor, which can control light that incidents onto a photodiode at various angles, and be suitable for a zoom function in a compact camera module by securing an incident angle margin, and a manufacturing method thereof are provided. The unit pixel of an image sensor includes: a first wafer including a photodiode containing impurities having an impurity type opposite to that of a semiconductor material and a pad for transmitting photoelectric charge of the photodiode to outside; a second wafer including a pixel array region in which transistors except the photodiode are arranged regularly, a peripheral circuit region having an image sensor structure except the pixel array, and a pad for connecting pixels with one another; and a connecting means connecting the pad of the first wafer and the pad of the second wafer. Accordingly, manufacturing processes can be simplified by constructing the upper wafer using only a photodiode and the lower wafer using the pixel array region except the photodiode, and costs are reduced since transistors are not included in the upper wafer portion, which in turn cannot affect the interaction with light.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Description

SEPARATION TYPE UNIT PIXEL OF 3-DIMENSIONAL IMAGE SENSOR AND MANUFACTURING METHOD THEREOF

Technical Field

[1] The present invention relates to a unit pixel of an image sensor, and more particularly, to a unit pixel of image sensor in which a photodiode is separated from a pixel array region and a manufacturing method thereof.

Background Art

[2] Pixels used in conventional image sensors are generally classified as 3-transistor pixels, 4-transistor pixels, or 5-transistor pixels according to the number of transistors included therein.

[3] FIGS. 1 to 3 show a typical pixel structure used for an image sensor, according to the number of transistors;

[4] FIG. 1 shows a 3-transistor structure. FIGS. 2 and 3 show a 4-transistor structure.

[5] As shown in FIGS. 1 to 3, a fill factor that is the area occupied by the photodiode over the entire area of the pixel is naturally reduced due to the existence of transistors in a pixel circuit,. In general, the fill factor of a diode ranges from 20 to 45%, considering capability of each semiconductor manufacturing process. Accordingly, light that is incident onto the rest area corresponding to about 55-80% of the entire area of the pixel is lost.

[6] To minimize the loss of optical data, a microlens is used for each unit pixel in a manufacturing process of the image sensor so that the optical data can be condensed onto the photodiode of each pixel. A microlens gain is defined as an increment of the sensitivity of a sensor using the microlens with respect to the sensitivity of the image sensor without the microlens.

[7] Given that the fill factor of a common diode is about 30's %, the microlens gain is 2.5-2.8 times of the sensitivity of the image sensor without the microlens. However, a pixel size has decreased to 4□×4□, and even to 3□×3□. Further, with an emergence of a small-sized pixel of 2.8□×2.8□ or 2.5□×2.5□, starting from when the pixel size is 3.4□×3.4□, the microlens gain significantly drops from 2.8 times to 1.2 times of the sensitivity of the image sensor without the microlens. This is caused by diffraction phenomenon of the microlens. The severity of diffraction phenomenon is determined by a function of a pixel size and a position of the microlens.

[8] As the pixel size gradually decreases, the severity of diffraction phenomenon of the microlens increases, thereby dropping the microlens gain equal to or less than 1.2 times of the sensitivity of the image sensor, which results in a phenomenon where the

light condensation seems to be unavailable. This is newly being recognized as a cause of sensitivity deterioration.

[9] In general, the decrease of the pixel size of the image sensor results in the decrease of the area of the photodiode. The area of the photodiode is closely related to the amount of available electric charge of the photodiode. Accordingly, the amount of available electric charge decreases when the size of the photodiode decreases. The amount of available charge of the photodiode is a basic factor for determining a dynamic range of the image sensor, and therefore the decrease of the amount of available electric charge directly affects the image quality of the sensor. When the image sensor of which the pixel size is less than 3.2□×3.2□ is manufactured, its sensitivity decreases, and the dynamic range of the sensor with respect to the light also decreases, thereby deteriorating the image quality.

[10] An external lens is used in the process of manufacturing a camera module using the image sensor. In this case, light is substantially perpendicularly incident onto a center portion of a pixel array. However, the light is less perpendicularly incident onto edge portions of the pixel array. When an angle starts to deviate from the vertical angle by a predetermined degree, the light is condensed onto the microlens which is out of the area pre-assigned for condensation of the photodiode. This generates a dark image, and more seriously, when the light is condensed onto a photodiode of an adjacent pixel, chromaticity may change.

[11] Recently, with the development of the image sensor having from 0.3 million pixels and 1.3 million pixel to 2 million pixels and 3 million pixels, a dynamic zoom-in/zoom-out function as well as an automatic focus function are expected to be included in a compact camera module.

[12] The features of the functions lie in that the incident angle of the light significantly changes at edge portions while each function is performed. The chromaticity or brightness of the sensor has to be independent of changes in the incident angle. With the decrease of the pixel size, the sensor cannot cope with the changes in the incident angle. At present, the sensor can support the automatic focus function, but the sensor can not support the dynamic zoom-in/zoom-out function. Therefore, it is difficult to develop a compact camera module providing a zoom function.

Disclosure of Invention

Technical Problem

[13] In order to solve the aforementioned problems, an object of the present invention is to provide a separation type unit pixel of an image sensor of which sensitivity drops far lesser than a conventional case in the manufacturing of a minute pixel, capable of controlling light incident onto a photodiode at various angles, and providing a zoom

function in a compact camera module by securing an incident angle margin, and a manufacturing method thereof.

Technical Solution

[14] According to an aspect of the present invention, there is provided a separation type unit pixel having a 3D structure for an image sensor including: a first wafer including a photodiode containing impurities having an impurity type opposite to that of a semiconductor material and a pad for transmitting photoelectric charge of the photodiode to outside; a second wafer including a pixel array region in which transistors except the photodiode are arranged regularly, a peripheral circuit region having an image sensor structure except the pixel array, and a pad for connecting pixels with one another; and a connecting means connecting the pad of the first wafer and the pad of the second wafer.

[15] According to another aspect of the present invention, there is provided a manufacturing method of a separation type unit pixel having a 3D structure for an image sensor, the method including: (a) constructing a first wafer including only a photodiode formed by implanting impurity ions into a semiconductor substrate; (b) constructing a second wafer including a pixel array region excluding the photodiode and a peripheral circuit region; (c) arranging the first wafer and the second wafer up and down for pixel array arrangement; (d) adhering a pad of a unit pixel on the first and second wafer arranged up and down; and (e) forming a color filter on the first wafer.

Brief Description of the Drawings

[16] FIGS. 1 to 3 show a structure of a pixel according to the number of transistors typically used for an image sensor;

[17] FIGS. 4 to 7 are circuit diagrams showing a structure of a separation type unit pixel for an image sensor, including a photodiode and four transistors, according to the present invention;

[18] FIGS. 8 to 11 are circuit diagrams showing a structure of a separation type unit pixel for an image sensor, including a photodiode and four transistors, according to an embodiment of the present invention;

[19] FIG. 12 shows a physical structure of a separation type unit pixel for an image sensor according to an embodiment of the present invention;

[20] FIG. 13 shows a physical structure of a separation type unit pixel for an image sensor according to another embodiment of the present invention;

[21] FIG. 14 shows a separation type unit pixel for a 3-dimensional image sensor according to an embodiment of the present invention;

[22] FIG. 15 shows a separation type unit pixel having a 3D structure for an image sensor according to another embodiment of the present invention;

[23] FIG. 16 is a flowchart of a method of manufacturing a separation type unit pixel having a 3D structure for an image sensor according to the present invention; and

[24] FIG. 17 shows a method of arranging a first wafer and a second wafer when manufacturing a separation type unit pixel having a 3D structure for an image sensor.

Best Mode for Carrying Out the Invention

[25] Hereinafter, the present will be described in detail with reference to accompanying drawings.

[26] FIGS. 4 to 7 are circuit diagrams showing a structure of a separation type unit pixel for an image sensor, including a photodiode and four transistors, according to the present invention, in which a photodiode region is separated from a pixel array region including four transistors.

[27] It is shown that a pixel array region having a four transistor (4T) structure including a transmission transistor, a reset transistor, a source follower transistor, and a selection transistor is separated from the photodiode.

[28] Here, methods of arranging the pixels having the 4T structure are various.

[29] A structure of the separation type unit pixel of the image sensor according to the present invention may be employed for N-type and P-type MOS transistors.

[30] FIGS. 8 and 9 are circuit diagrams showing a structure of a separation type unit pixel for an image sensor according to an embodiment of the present invention in which a photodiode region is separated from a pixel array region including three transistors.

[31] It is shown that the pixel array region having a three transistor (3T) structure including a reset transistor, a source follower transistor and a selection transistor is separated from the photodiode.

[32] FIGS. 10 and 11 are circuit diagrams showing a structure of a separation type unit pixel for an image sensor according to another embodiment of the present invention.

[33] It is shown that a region where the photodiode and the reset transistor are formed is separated from a pixel array region where the rest of the transistors except the reset transistor in the 3T structure are formed.

[34] Here, methods of arranging the pixels having the 3T structure are various. A structure of the separation type unit pixel of the image sensor according to the present invention may be employed for N-type and P-type MOS transistors.

[35] FIG. 12 shows a physical structure of a separation type unit pixel for an image sensor according to an embodiment of the present invention which includes first and second wafer 10 and 20.

[36] The first wafer 10 includes the photodiode 14 having a P-type semiconductor structure by implanting impurities into a semiconductor substrate and a pad 17

transmitting photoelectric charge of the photodiode 14 to outside.

[37] The second wafer 20 includes a pixel array region where the circuit elements except the photodiode including transistors are regularly arranged, a peripheral circuit region, and a pad 21 connecting pixels with one another.

[38] In the pixel array region, the rest of the circuit elements constituting a pixel (i.e., a transmission transistor 22, a reset transistor 23, a source follower transistor 24 and/or a selection transistor 25) are regularly arranged. In the peripheral circuit region, a circuit for reading a signal of the image sensor, a correlated double sampling (CDS) circuit, a circuit for processing a general analogue signal, other digital control circuit, and a digital circuit for processing an image signal are included.

[39] FIG. 13 shows a physical structure of a separation type unit pixel for an image sensor according to another embodiment of the present invention in which the second wafer 20 has a 3T structure.

[40] Specifically, in the pixel array region of the second wafer 20, the rest of the circuit elements constituting a pixel (i.e., a reset transistor 23, a source follower transistor 24 and/or a selection transistor 25) are regularly arranged.

[41] FIG. 14 shows a separation type unit pixel having a 3D structure for an image sensor according to an embodiment of the present invention in which the first wafer 10 is separated from the second wafer 20.

[42] The first wafer 10 includes a color filter 12 and the photodiode 14.

[43] The second wafer 20 includes a pixel array region where elements including transistors are regularly arranged and a peripheral circuit region constituting an image sensor structure including the rest of the pixel elements except the pixel array.

[44] The first and second wafer 10 and 20 are connected to conductor layers 17 and 21 for external connection.

[45] The first wafer portion 10 will now be described in detail.

[46] The first wafer 10 includes the color filter 12 allowing each pixel to display a specific color, a semiconductor material 13 containing specific impurities used to form the photodiode 14, a first transparent buffer layer 18 to be inserted between the color filter 12 and the semiconductor material 13 so as to facilitate the formation of structures and improve the light transmittance, and the photodiode containing impurities having an impurity type opposite to that of the semiconductor material 13.

[47] In addition, a conductor pad 17 for external connection is formed in the first wafer portion 10 according to the present invention.

[48] The second wafer portion 20 will now be described in detail.

[49] The second wafer portion 20 is divided into the pixel array region having a 3T or 4T structure and the peripheral circuit region. The peripheral circuit region has a typical image sensor structure. Accordingly, the peripheral circuit region may include a

circuit for reading an image sensor signal, a CDS circuit, a circuit for processing a common analog signal, a digital control circuit, and an image signal processing digital circuit.

[50] In the pixel array region, pixel elements except the photodiode which constitute the pixel are regularly arranged. An example of this is shown in the lower part of FIG. 12. First, the pixel array region includes a conductor pad 21 for receiving a signal from the upper part of the pixel array region, a reset transistor for initializing the photodiode 14, a source follower transistor 24 for transmitting voltage statuses of a voltage source VDD and a floating diffusion region 15, that is a floating node, to outside, a selection transistor 25 for controlling connection between a pixel and an external lead-out circuit to transmit information of the pixel, and an output electrode 26 of the pixel.

[51] FIG. 15 shows a separation type unit pixel for a 3-dimensional image sensor according to another embodiment of the present invention.

[52] The unit pixel of FIG. 15 further includes a microlens 11 condensing light onto the photodiode and a second transparent buffer layer 19 which is inserted to facilitate the formation of structures and improve the light transmittance. The second transparent buffer layer 19 is additionally used and corresponds to the membrane of a common image sensor.

[53] FIG. 16 is a flowchart of a manufacturing method of a separation type unit pixel having a 3-dimensional structure for an image sensor according to the present invention.

[54] First, a first wafer is constructed with only a photodiode formed by implanting impurity ions into the semiconductor substrate (operation S611).

[55] In the process of constructing the first wafer portion, a second wafer portion is constructed to have the pixel array region including a transmission transistor, a reset transistor, a source follower transistor, and a blocking switch transistor and the peripheral circuit region including a lead-out circuit, a vertical/horizontal decoder, a CDS circuit which involves in a sensor operation and an image quality, and analog circuit, an analog-digital converter (ADC), and a digital circuit (operation S612).

[56] Second, the first wafer and the second wafer are arranged up and down (operation S620).

[57] To arrange the first wafer and the second wafer up and down, the wafer portions may be arranged in an optical manner by making a hole in the first wafer by using an infrared ray (IR) penetrating method, an etching method, or a laser punching method.

[58] In the IR penetrating method, the wafer are disposed without making a hole in the first wafer. In the etching method or the laser punching method, a hole is formed through the first wafer, and then the wafer are arranged through optical pattern recognition.

[59] Third, the first and second wafer arranged up and down are adhered to a conductor pad (operation S630).

[60] Fourth, the surface thickness of the back side of the first wafer portion is reduced to form thin back side of the first wafer (operation S640).

[61] After the first wafer is adhered to the second wafer, the back side of the first wafer is thinned to reduce the wafer thickness. In order to reduce the thickness of the back side of the first wafer, the back side of the wafer is processed by a grinding process, a chemical mechanical polishing (CMP) process, or an etching process.

[62] Fifth, a color filter is formed on the first wafer (operation S650).

[63] Sixth, a microlens is formed on the color filter (operation S660).

[64] FIG. 17 shows an arrangement of the first and second wafer when manufacturing a separation type unit pixel having a 3D structure for an image sensor, according to an embodiment of the present invention.

[65] The first and second wafer 10 and 20 are accurately aligned by using the IR penetrating method, the etching method, or the laser punching method.

[66] In FIG. 17, a hole is formed through the first wafer 10 by using the etching method or the laser punching method.

[67] The hole is not formed through the first wafer in using the IR penetrating method.

[68] The manufacturing method of a separation type unit pixel having a 3D structure for an image sensor of the present invention is not limited to a CMOS manufacturing process, and the method may be used in other semiconductor manufacturing processes.

[69] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.

Industrial Applicability

[70] Accordingly, the present invention has advantages in that, manufacturing processes can be simplified by constructing the upper wafer using only a photodiode and the lower wafer using the pixel array region except the photodiode, and costs are reduced since transistors are not included in the upper wafer, which in turn cannot affect the interaction with light.

[71] In addition, the present invention has advantages in that, by forming an area for a photodiode almost the same as an area for a pixel, an image sensor can be manufactured to have a good sensitivity in a subminiature pixel, without a microlens. In addition, by disposing the photodiode at the top layer, an incident angle margin of incident light can be secured, which has to be basically provided by the sensor for its

auto focusing function or zoom function.

Claims

[1] A separation type unit pixel having a 3D structure for an image sensor comprising:
a first wafer including a photodiode containing impurities having an impurity type opposite to that of a semiconductor material and a pad for transmitting photoelectric charge of the photodiode to outside;
a second wafer including a pixel array region in which transistors except the photodiode are arranged regularly, a peripheral circuit region having an image sensor structure except the pixel array, and a pad for connecting pixels with one another; and
a connecting means connecting the pad of the first wafer and the pad of the second wafer.

[2] The separation type unit pixel having a 3D structure for an image sensor of claim 1, wherein the first wafer comprises:
a semiconductor material which contains specific impurities for forming a photodiode;
a first transparent buffer layer which is inserted between the color filter and the semiconductor material to facilitate the formation of structures and to improve light transmittance;
a photodiode which contains impurities having an impurity type opposite to that of the semiconductor material; and
a pad transmitting photoelectric charge of the photodiode to outside.

[3] The separation type unit pixel having a 3D structure for an image sensor of claim 2, wherein the first wafer comprises:
a color filter which allows each pixel to display a specific color;
a microlens which collects light to be condensed onto the photodiode; and
a second transparent buffer layer which is inserted between the microlens and the color filer to facilitate the formation of structures and to improve light transmittance.

[4] The separation type unit pixel having a 3D structure for an image sensor of claim 1, wherein, in the pixel array region of the second wafer, the rest of the circuit elements constituting a pixel such as a transmission transistor, a reset transistor, a source follower transistor, and/or a blocking switch transistor are arranged regularly.

[5] The separation type unit pixel having a 3D structure for an image sensor of claim 1, wherein the peripheral circuit region comprises a circuit for extracting an image sensor signal, a CDS circuit, a circuit for processing a common analog

signal, a digital control circuit, and an image signal processing digital circuit.

[6] A manufacturing method of a separation type unit pixel having a plurality of transistors for an image sensor, the method comprising:

(a) constructing a first wafer with only a photodiode formed by implanting impurity ions into a semiconductor substrate;

(b) constructing a second wafer including a pixel array region except the photodiode and a peripheral circuit region;

(c) arranging the first wafer and the second wafer up and down for pixel array arrangement;

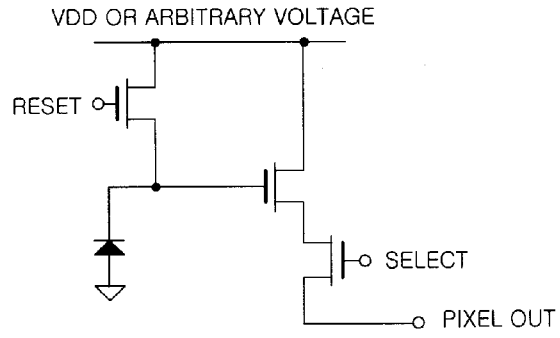
(d) adhering a pad of a unit pixel on the first and second wafer arranged up and down; and

(e) forming a color filter on the first wafer.

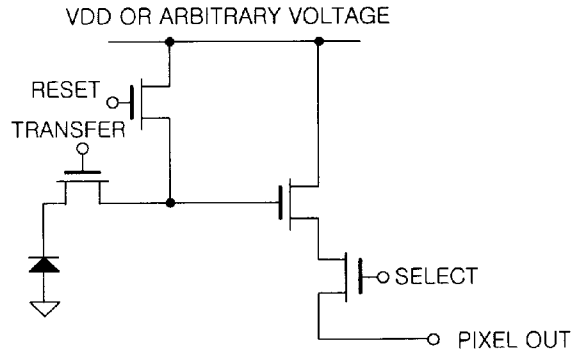
[7] The method of claim 6, further comprising (f) forming a microlens on the color filter to condense light.

[8] The method of claim 6 or 7, further comprising performing surface processing for thinning the back side of the first wafer to reduce the thickness of the back side of the first wafer.

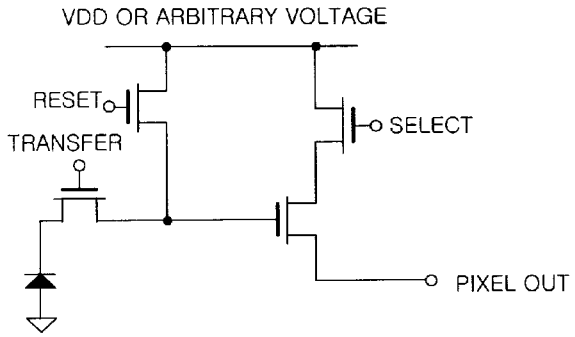
[Fig. 1]



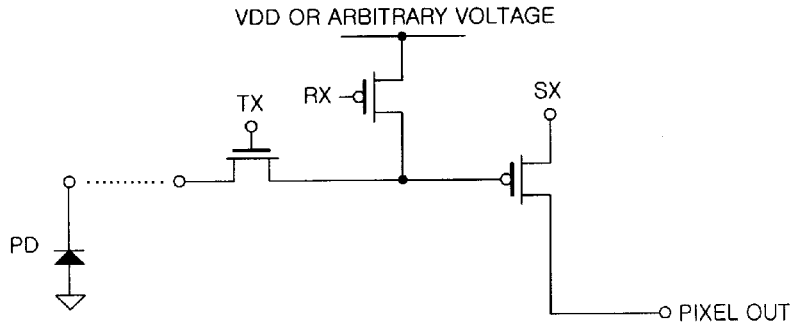
[Fig. 2]



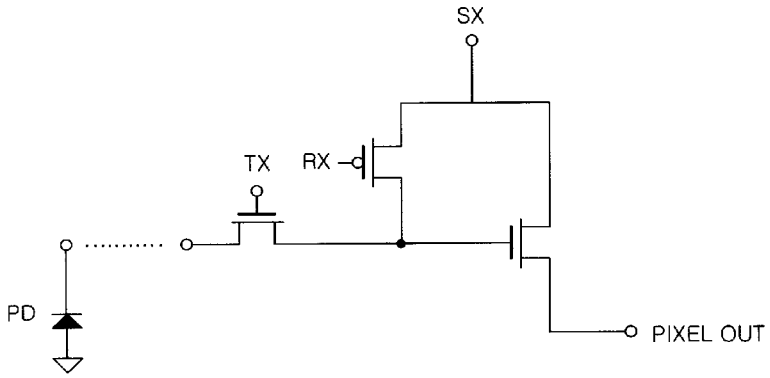
[Fig. 3]



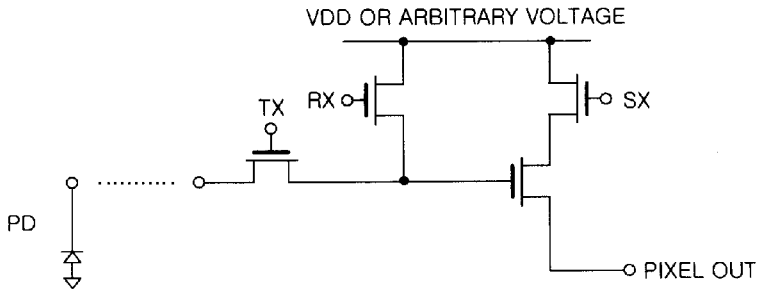
[Fig. 4]



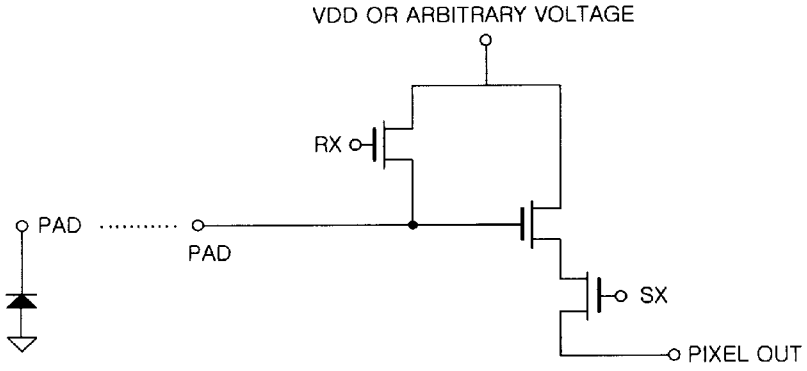
[Fig. 5]



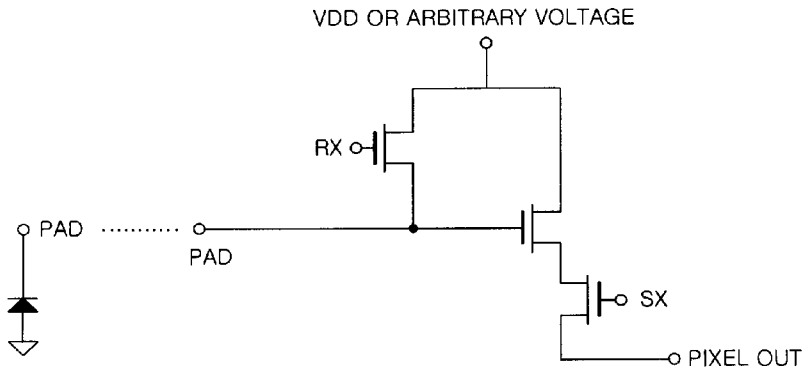
[Fig. 6]



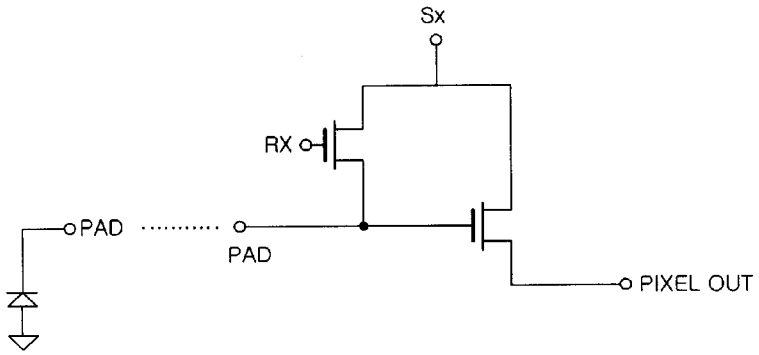
[Fig. 7]



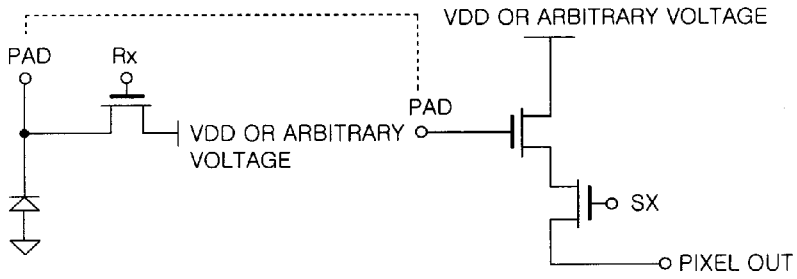
[Fig. 8]



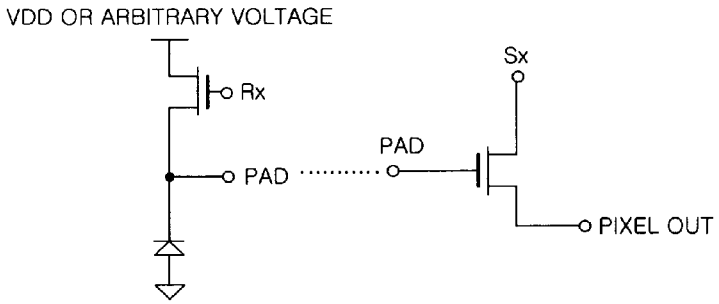
[Fig. 9]



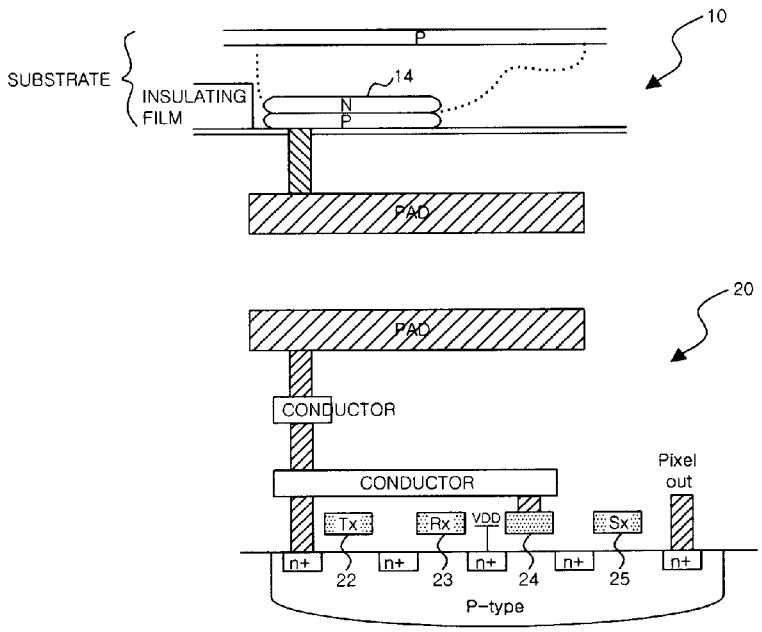
[Fig. 10]



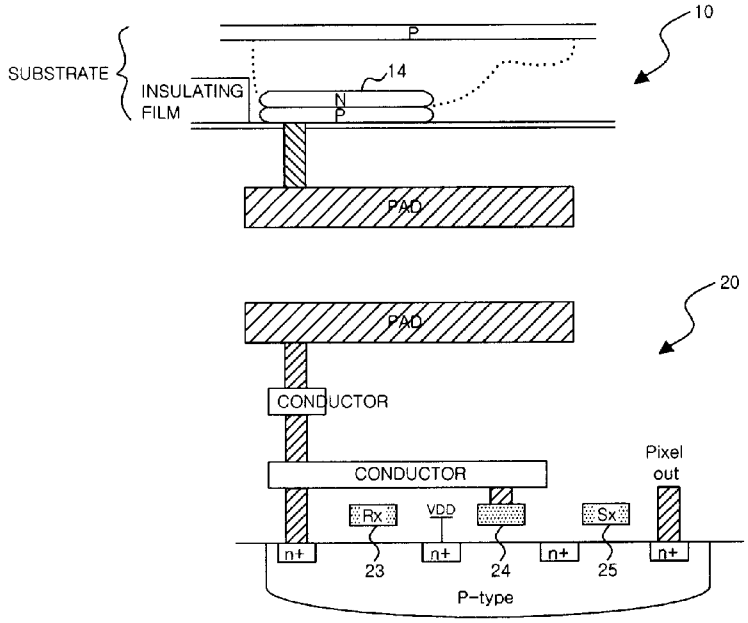
[Fig. 11]



[Fig. 12]



[Fig. 13]


10
P
SUBSTRATE
INSULATING FILM
14
N
P
PAD
20
PAD
CONDUCTOR
CONDUCTOR
Pixel out
Rx
VDD
Sx
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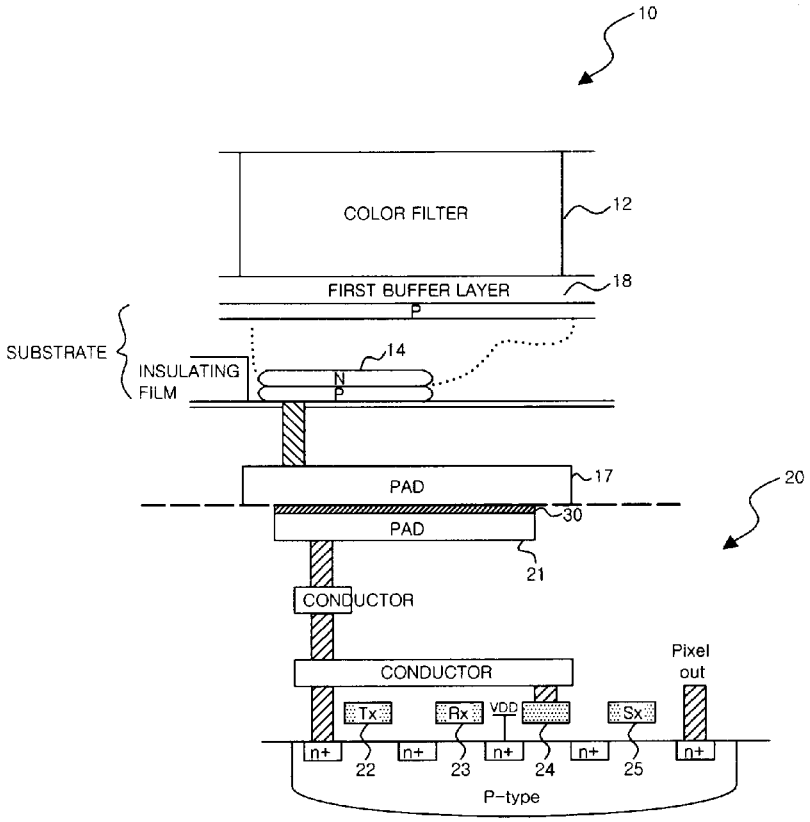
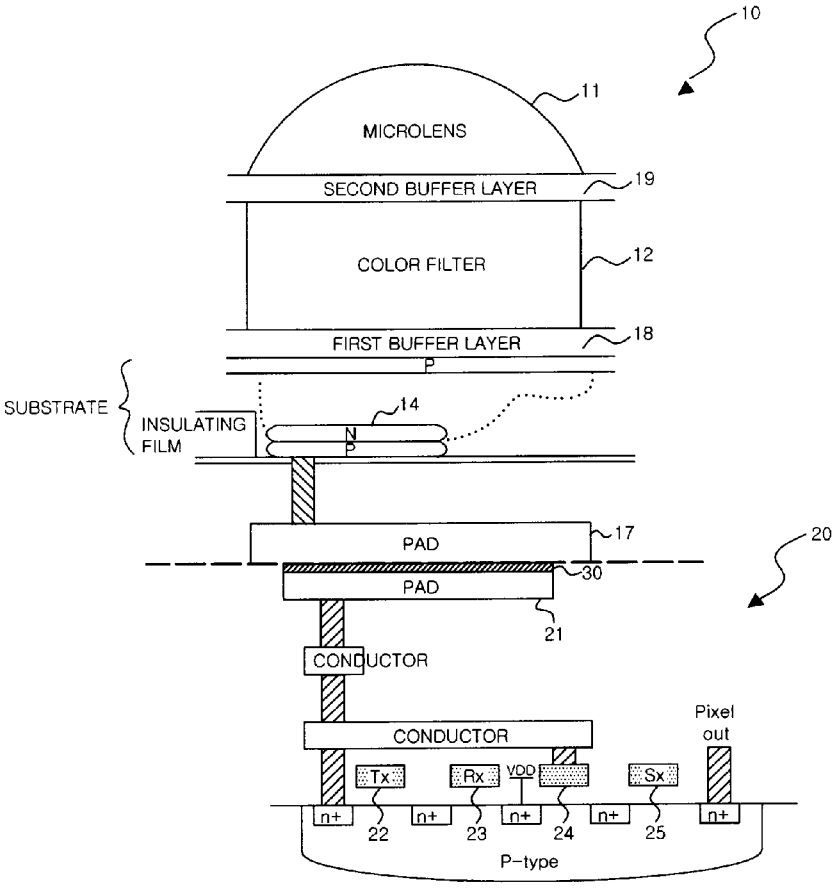
24
25
P-type

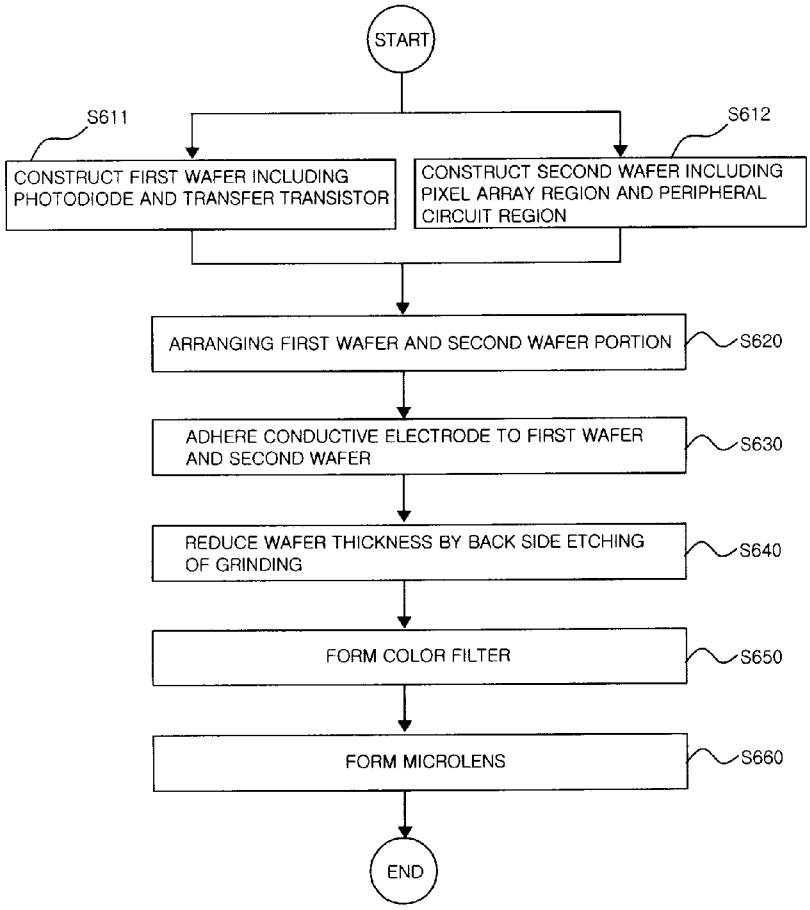
[Fig. 14]


10
COLOR FILTER
12
FIRST BUFFER LAYER
18
P
SUBSTRATE
INSULATING FILM
14
N
P
PAD
17
20
PAD
30
21
CONDUCTOR
CONDUCTOR
Pixel out
Tx
Rx
VDD
Sx
n+
22
23
24
25
P-type

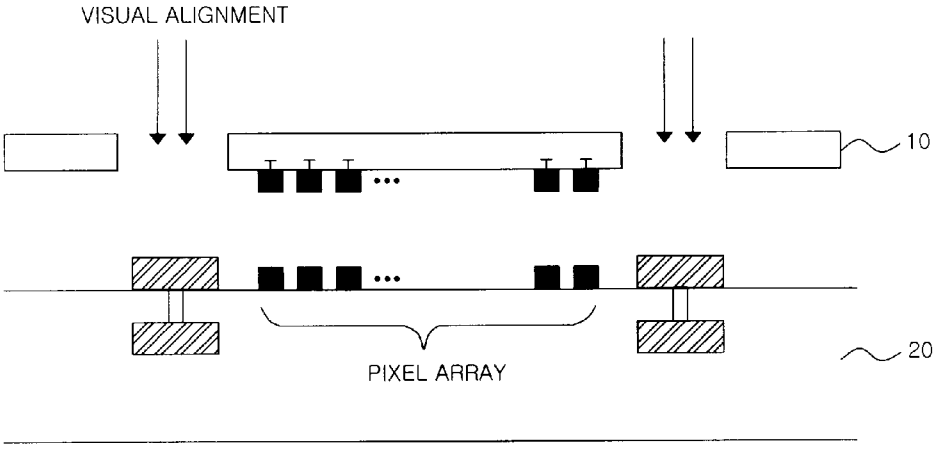
[Fig. 15]


10
11
MICROLENS
SECOND BUFFER LAYER
19
COLOR FILTER
12
FIRST BUFFER LAYER
18
P
SUBSTRATE
INSULATING FILM
14
N
P
PAD
17
20
PAD
30
21
CONDUCTOR
CONDUCTOR
Pixel out
Tx
Rx
VDD
Sx
n+
22
n+
23
n+
24
n+
25
n+
P-type

[Fig. 16]


START
S611
S612
CONSTRUCT FIRST WAFER INCLUDING PHOTODIODE AND TRANSFER TRANSISTOR
CONSTRUCT SECOND WAFER INCLUDING PIXEL ARRAY REGION AND PERIPHERAL CIRCUIT REGION
ARRANGING FIRST WAFER AND SECOND WAFER PORTION
S620
ADHERE CONDUCTIVE ELECTRODE TO FIRST WAFER AND SECOND WAFER
S630
REDUCE WAFER THICKNESS BY BACK SIDE ETCHING OF GRINDING
S640
FORM COLOR FILTER
S650
FORM MICROLENS
S660
END

[Fig. 17]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2006/002482

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/146(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Patents and applications for inventions since 1975
Korean Utiltiy models and applications for Utility models since 1975
Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) : "wafer level", "image sensor", "stack", "align"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US6486522 B1 (Pictos Technologies, Inc) 26 NOVEMBER. 2002 See the abstracts, figures 2, 5 and column 1, line 25 - column 1, line 32, column 4, line 34 - column 4, line 36	1-8
Y	A.R.Mirza, ' One Micron Precision, Wafer-Level Aligned Bonding for Interconnect, MEMS and Packaging Applications' in : 2000 Electronic Components and Technology Conference, PP 676-680.	1-8
A	JP 2003-273343 A (SONY CORP) 26 SEPTEMBER 2003 see the abstract, figure 7-10 and [0033]-[0045] of specification	3, 6-8
A	US 06642081 B1 (Robert Patti) 4 NOVEMBER 2003 see the abstract, figure 1 and column 3, line 45 - column 4, line 46	1-8

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 SEPTEMBER 2006 (25.09.2006)	**25 SEPTEMBER 2006 (25.09.2006)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2006/002482

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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JP 2003-273343 A	26.09.2003	JP3722367 B	30.11.2005
		US2004-0005729 A1	08.01.2004
		US2005-05690 2 A1	17.03.2005
		US6821809 B	23.11.2004
US 06642081 B1	04.11.2003	US2003193076A1	16.10.2003
		US2004048459A1	11.03.2004
		US6838774BB	04.01.2005