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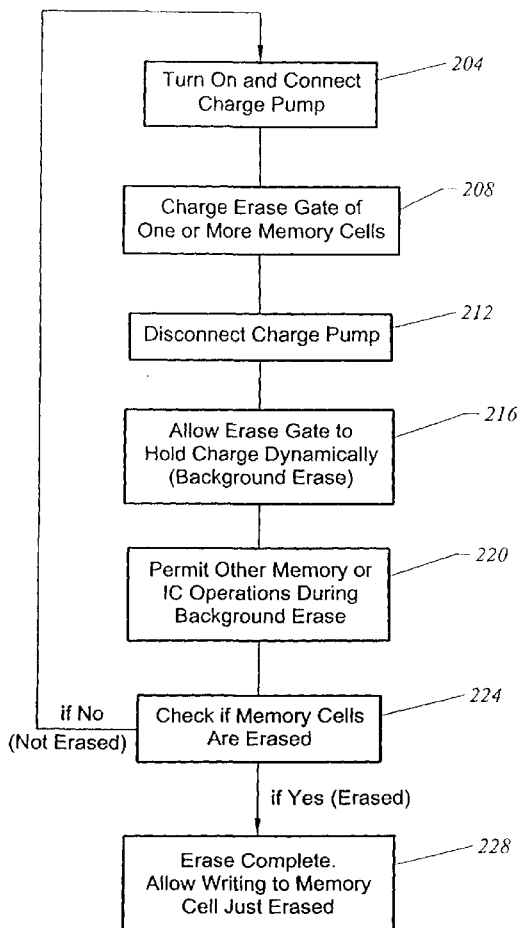
(43) International Publication Date  
27 March 2003 (27.03.2003)

(10) International Publication Number  
**PCT**  
**WO 03/025937 A3**

- (51) International Patent Classification<sup>7</sup>: G11C 16/16, 8/08
- (21) International Application Number: PCT/US02/29554
- (22) International Filing Date:  
17 September 2002 (17.09.2002)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
09/956,201 17 September 2001 (17.09.2001) US
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- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: BACKGROUND OPERATION FOR MEMORY CELLS



(57) Abstract: A technique to perform an operation (e.g., erase, program, or read) on memory cells (105) is to apply an operating voltage dynamically to the gates (111, 113) of the memory cells, rather than a continuous operating voltage. This reduces the power consumed during the operation. Dynamic operation or background operation such as background erase also permits other operations, such as read, program, or erase, to occur while the selected memory cells are operated on. This improves the operational speed of an integrated circuit using dynamic operation compared to a continuous operation. In an embodiment for background erase, the erase gates are charged to the erase voltage using a charge pump (204, 208). The pump is then turned off (212), and the erase gates remain at the erase voltage dynamically (216). The erase voltage at the erase gates will be periodically checked and refreshed as needed until the memory cells are fully erased (224). While the charge pump is off and the erase voltage is dynamically held at the erase gates, other operations, possibly on other memory cells, may be performed (220).



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**Declaration under Rule 4.17:**

— *of inventorship (Rule 4.17(iv)) for US only*

**Published:**

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

**(88) Date of publication of the international search report:**

27 November 2003

# INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 02/29554

**A. CLASSIFICATION OF SUBJECT MATTER**  
 IPC 7 G11C16/16 G11C8/08

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
 IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages                                 | Relevant to claim No.      |
|------------|--|----------------------------|
| X<br>A     | US 5 949 716 A (SO HOCK C ET AL)<br>7 September 1999 (1999-09-07)<br>column 2, line 7 - line 10<br>-----           | 10-14<br><br>1-9,<br>15-23 |
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| X          | US 5 959 887 A (TAKASHINA NOBUAKI ET AL)<br>28 September 1999 (1999-09-28)<br>column 5, line 23 - line 27<br>----- | 10-14                      |

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Date of the actual completion of the international search

16 September 2003

Date of mailing of the international search report

29/09/2003

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# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 02/29554

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s) | Publication<br>date |            |
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