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(71) Applicant: ELECTRONIC ARTS, INC. [US/US]; 1450 Fashion Island Boulevard, San Mateo, CA 94404 (US).

(72) Inventors: FOWLER, Terry; 387 Foxborough, Mountain View, CA 94041 (US). McGRATH, Kevin; 299 Lansing Way, Hayward, CA 94541 (US). GOODE, Terry, Lee; 1390 Sage Hen, Sunnyvale, CA 94087 (US). SCHNECKLOTH, Mark; 5018 Parkfield, San Jose, CA 95129 (US).

(74) Agents: TRUONG, Phong, K. et al.; Fenwick & West, Suite 500, Two Palo Alto Square, Palo Alto, CA 94306 (US).

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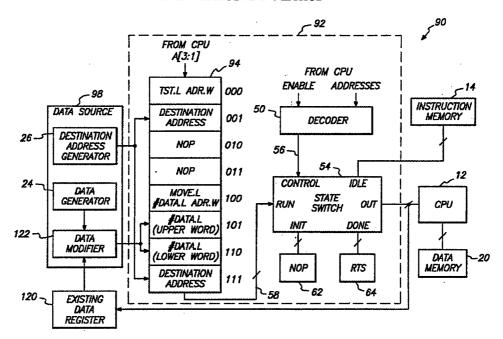
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(54) Title: DATA TRANSFER ACCELERATING APPARATUS AND METHOD



In a computing system, data is transferred from a data source (18) to a memory (20) by generating and sending an optimized instruction sequence to a central processing unit (CPU 12). The CPU (12) executes the instruction sequence to carry out the data transfer in an optimal manner. An apparatus for carrying out the above method comprises a determiner (50), an instruction generator (52), and a coupling circuit (54). The determiner (50), in response to a determination that data transfer is desired, generates a run control signal. The instruction generator (52) generates an optimized instruction sequence using data and address information received from the data source (18), and provides this instruction sequence on its output. The coupling circuit (54), in response to the run control signal, relays the optimized instruction sequence from the instruction generator (52) to the CPU (12) to allow the CPU (12) to execute the instruction set to transfer data from the data source (18) to the memory (20).

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# INTERNATIONAL SEARCH REPORT

li national application No. PCT/US94/09604

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US CL : 39	95/375					
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