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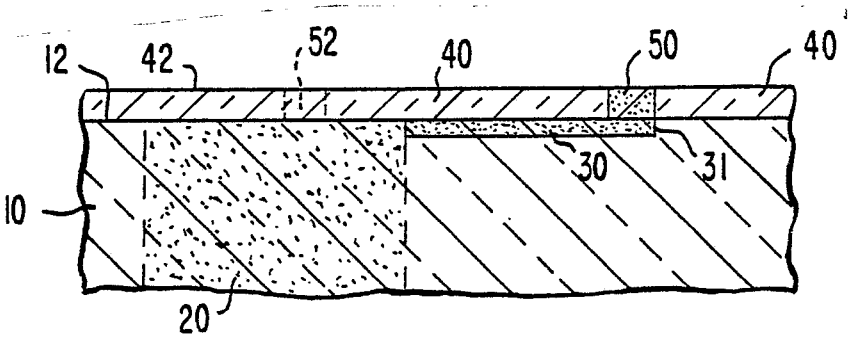

(57) Abstract

A method and structure for reducing the surface area occupied by feedthrough in a semiconductor substrate. A buried horizontal conducting path (30) is laid down on a major surface (12) of a substrate (10), with one end (32) of the conducting path (30) in electrical and physical contact with the feedthrough (20) (e.g. a thermal gradient zone melt TGZM). An epitaxial layer (40) is put down over the TGZM and over the buried horizontal conducting path (30). Electrical contact is made to the distal end (31) of the buried horizontal conducting path (30) by diffusion through the newly put down epitaxial layer (40) or by etching to the conducting path. The diffused region (50) is of the same dopant characteristics and conductivity type as are the horizontal path (30) and TGZM. The cross-sectional area of the diffusion region (50) is 25 to 30 square microns compared to the 507 to 2027 square microns area of the TGZM. This results in substantial reduction of the surface area occupied by feedthrough structures and allows more devices to be fabricated on the surface of the substrate.

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FEEDTHROUGH STRUCTURE FOR THREE DIMENSIONAL MICROELECTRONIC DEVICES

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to the structure of semiconductor devices and particularly to the structure of microelectronic feedthroughs for three dimensional circuits.

2. Description of the Prior Art

Feedthrough structures generally are well known. A common form of feedthrough is the thermal gradient zone melt (TGZM). For additional information on the TGZM process, one is referred to the following U.S. patents: Method of Making Deep Diodes, 3,901,736; Deep Diode Device and Method, 3,902,925; Deep Diode Devices and Method and Apparatus, 4,075,038; High Velocity Thermomigration Method of Making Deep Diodes, 3,898,106; The Stabilized Droplet Method of Making Deep Diodes Having Uniform Electrical Properties, 3,899,361; Method of Making Isolation Grids in Bodies of Semiconductor Material, 3,904,442; and Thermomigration of Metal-Rich Liquid Wires Through Semiconductor Materials, 3,899,362. Feedthroughs effected by the TGZM process typically have a cross sectional area on the order of one to two mils in diameter. Since no devices can be fabricated on the semiconductor surface occupied by the feedthrough, the presence of the feedthrough reduces the number of

devices that can be placed on the semiconductor surface This result is contrary to the everpresent objective to increase the number and density of devices fabricated on a semiconductor device.

It is therefore an object of the present invention to minimize the surface area of a semiconductor which is occupied by feedthrough structure, thereby permitting an increase in the density, and number, of devices which can be fabricated on the surface.

SUMMARY OF THE INVENTION

The invention comprises a method and structure for reducing the surface area occupied by the end of the verticle feedthrough in a three dimensional semiconductor circuit device. A horizontal conducting path is laid down on a major surface of the substrate, with one end of the conducting path in electrical and physical contact with the feedthrough (e.g. a thermal gradient zone melt, TGZM). An epitaxial layer is then put down over the major surface covering the TGZM and burying the horizontal conducting path. Electrical contact is made to the other end of the buried horizontal conducting path by diffusion through the newly put down epitaxial layer, or by etching through the new epitaxial layer to the conducting path. The diffused region is of the same conductivity type as are the horizontal buried path and the TGZM. The cross sectional area of the diffusion region is 25 to 30 square microns compared to the 507 to 2027 square microns area of the TGZM. This results in substantial reduction of the surface area occupied by the ends of the TGZM feedthrough structure and allows more devices to be fabricated on the major surface of the semiconductor.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a cross-sectional view of a section of a semiconductor substrate.

FIG. 2 illustrates the placement of a feedthrough in the substrate.

FIG. 3 shows the horizontal conducting means contacting one end of the feedthrough.

FIG. 4 shows the addition of a thin epitaxial layer covering the feedthrough and horizontal conducting means.

FIG. 5 shows the electrical connection between the horizontal conducting means and the top surface of the epitaxial layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

To meet the ever increasing packaging density demanded in various applications of semiconductor electronics the semiconductor industry has begun to fabricate rather sophisticated devices by stacking multiple substrates one on top of the other. Such circuits are often referred to as three-dimensional devices. Electrical connections are frequently made between the devices on one substrate and devices on another substrate. This interconnection is accomplished by a feedthrough structure. A feedthrough is an electrically conductive path which extends vertically through the substrate substantially perpendicular to the major surfaces of the substrate.

FIG. 1 shows a cross section of a small portion of semiconductor substrate 10. The substrate 10 has a first or top major surface 12 and a second or bottom major surface 14. Such a substrate may be stacked with others like it to form a high density three dimensional semiconductor device. Also, active devices may be fabricated on both major surfaces 12 and 14 of

substrate 10. In both cases it is often desirable to electrically connect a device on one substrate with a device on another substrate or to connect a device on a top major surface such as 12 with a device on a bottom major surface such as 14. Such interconnection is facilitated by the structure 20, as shown in FIG. 2, which comprises an electrically conductive path called a feedthrough. The feedthrough extends from one major surface 12 through the semiconductor substrate 10 to the other major surface 14. A semiconductor device on surface 12 may be electrically connected to a semiconductor device on surface 14 by connecting the first device to the end 22 of feedthrough 20 lying on surface 12 and connecting the other device to the end 24 of feedthrough 20 which lies on surface 14. Such an interconnect is well known and described in the earlier referenced literature.

While the feedthrough structure is a convenient means to interconnect devices on opposite sides of a substrate, it does have the disadvantage of occupying substantial space on the major surfaces 12 and 14. Devices cannot be fabricated in the area occupied by the feedthrough nor in the small annular area surrounding the feedthrough. The total space lost can be significant if a number of feedthroughs are present in a single wafer. Typically the feedthrough 20 will have a diameter of from 1 to 2 mils, i.e. an area of about 507 square microns to about 2027 square microns.

The amount of surface area occupied by feedthrough structure and hence unavailable for fabrication of circuit devices, can be significantly reduced by the method and structure illustrated in FIGS. 3, 4 and 5.

First a shallow conducting means such as conducting path 30 is fabricated in surface 12. The path 30 can be as long as desired and practical and the path may terminate in end 31 wherever convenient and compatible with the contemplated circuit. One end of path 30 must contact feedthrough 20 as shown at 32. The path 30 is electrically conductive, and of the same conductivity type as is feedthrough 20.

Next, a thin epitaxial layer 40 is applied as illustrated in FIG. 4 to cover the major surface 12, the end 22 of feedthrough 20, and the conducting path 30. Epitaxial layer 40 is of the same conductivity type as is substrate 10, and is relatively thin. The layer 40 may range from 0.5 to 20.0 microns in thickness.

Finally, a conductive path 50 as shown in FIG. 5 is fabricated and extends from surface 42 to path 30. This path 50 may be formed by diffusion through the epitaxial layer 40. Path 50 is of the same conductivity as the TGZM and of opposite conductivity as the substrate 10. Typically, path 50 may be 5 microns square covering an area of about 25 square microns. This represents a significant decrease from the area of surface 12 occupied by the TGZM which was from 507 to 2027 square microns. The surface area of layer 40, located directly above feedthrough 20, is available for fabrication of semiconductor devices.

As shown in FIG. 5, the conductive path 50 is located at the distal end 31 of conductive path 30. With this configuration, path 30 could be tailored to place conductive path 50 at any desired location. Specifically, all paths 30 on a given substrate could be made to terminate near the perimeter of the substrate. All paths 50 would correspondingly be located near the perimeter of the substrate, leaving the interior area of the substrate totally free of feedthrough connections. If preferred for a particuar application, paths 30

could be eliminated and paths 50 could be formed through layer 40 directly above (or below) the end 22 (or 24) of feedthrough 20. Such a path is shown as path 52 shown in broken lines in FIG. 5. In either case, the percentage of the surface area of surface 42 which is occupied by feedthrough structure is drastically reduced from the percentage of the surface area of surface 12 which is occupied by feedthrough structure. The percentage reduction can be on the order of $\frac{2002}{2027}$ or 98.7%.

Whenever a feedthrough such as 20 is formed in a substrate 10, microscopic structural defects appear in the substrate 10 immediately surrounding the feedthrough 20. These defects effectively increase the area of surface 12 which is unsuited for fabrication of devices. Thus, as a design rule of thumb, it is typical that no devices are fabricated closer than about 25 microns from the feedthrough. The percentage improvement noted above is thus a conservative figure. Because the layer 40 covers over and fills in these defects, it is expected that the above discussed method will improve the net yield of substrates utilizing the TGZM process.

Typically the substrate 10 will be 10 to 20 mils thick and comprised of a semiconductor of any type IV, type III-V, or type II-VI compound. To produce well controlled feedthroughs, the crystal orientation in silicon is normally <100> for the feedthrough direction. Thus the major surfaces 12 and 14 are <100> oriented surfaces.

While the invention has been described with particular reference to FIGS. 1 through 5, the figures and description are for purposes of illustration only and are not to be interpreted as limitations upon the invention. Many changes in material and structure may be made by one having ordinary skill in the art, without departing from the spirit and scope of the invention.

As an example, conductive path 50 (and 52) shown extending from surface 42 to path 30 (or to feed-through 20) is shown as a diffused region. The conductive paths 50 or 52 could also be formed by etching through layer 40 by conventional techniques and providing a conductor also by conventional techniques, from surface 42 to path 30 (or feed-through 20). The spirit and scope of the invention are intended to be limited only by the appended claims.

CLAIMS

What is Claimed is:

1. In a semiconductor substrate having a first major surface and a second major surface and a feedthrough structure extending through said substrate from said first major surface to said second major surface, the improvement comprising:

an epitaxial layer, of the same conductivity type as said substrate, applied to at least one of said first and second major surfaces covering said feedthrough structure and forming a new major surface; and

a first conductive path of the same conductivity type as said feedthrough structure formed in said epitaxial layer and extending from said new major surface to the underlying major surface of said substrate;

said first conductive path being in electrical communication with said feedthrough structure and having a cross-sectional area substantially less than the cross-sectional area of said feedthrough structure.

2. The improvement according to Claim 1 further comprising a second conductive path having a first end and a second end:

said first end joining said second path to said feedthrough structure and said second end joining said second path to said first path;

whereby said first path is in electrical communication with said feedthrough structure.

3. The improvement according to Claim 1 or Claim 2 wherein said feedthrough structure is formed by the thermal gradient zone melt process.

4. The improvement according to Claim 1 or Claim 2 wherein said first conductive path is formed by diffusion.

5. A method for reducing the surface area occupied by the feedthrough structure of a semiconductor substrate comprising the steps of:

applying a relatively thin epitaxial layer of the same conductivity type as said substrate to a major surface of said substrate so as to cover said feedthrough structure and form a new major surface;

forming an electrically conductive path through said epitaxial layer and extending from said new major surface to the underlying major surface of said substrate;

said electrically conductive path being in electrical communication with said feedthrough structure.

6. A method for reducing the surface area occupied by the feedthrough structure of a semiconductor substrate comprising the steps of:

forming a first electrically conductive path in a major surface of said substrate, said first electrically conductive path having a first end joining said feedthrough structure and a second end located remote from said feedthrough structure;

applying a relatively thin epitaxial layer, of the same conductivity type as said substrate, to said major surface so as to cover said feedthrough structure and said first electrically conductive path and forming a new major surface; and

forming a second electrically conductive path through said epitaxial layer and extending from said new major surface to the underlying second end of said first electrically conductive path; with the cross-sectional area of said second electrically conductive path being much less than that of the feedthrough structure;

whereby said second electrically conductive path is in electrical communication with said feedthrough structure and occupies less area of said new major surface than said feedthrough structure occupied of the original uncovered major surface of said substrate.

7. The method of Claim 6 wherein said second electrically conductive path is formed by diffusion.

Fig. 1.

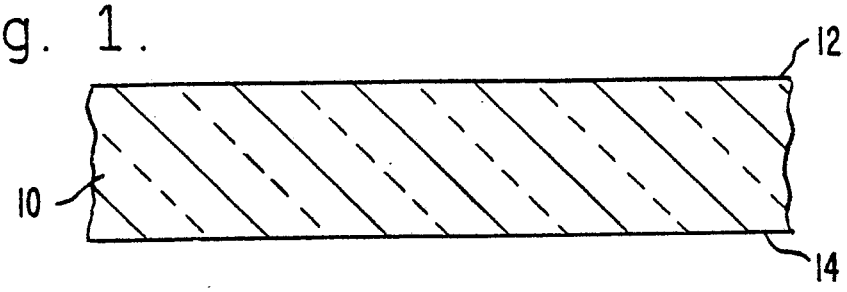


Fig. 2.

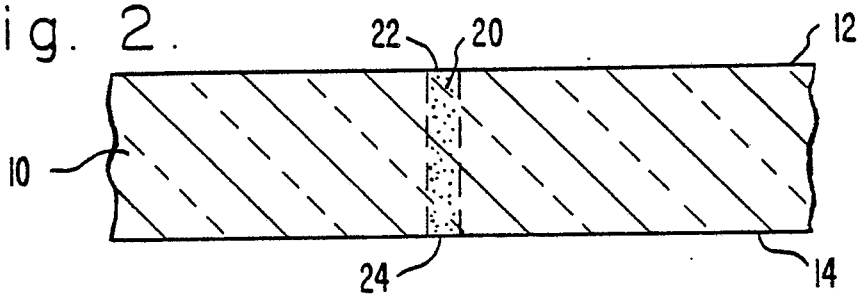


Fig. 3.

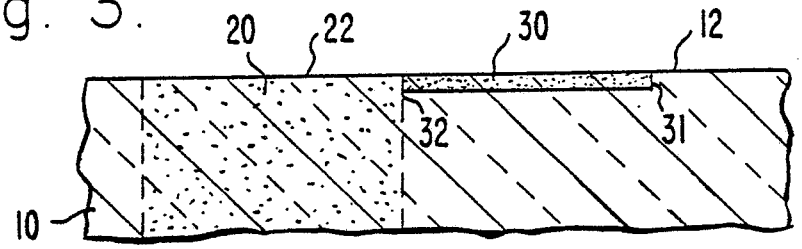


Fig. 4.

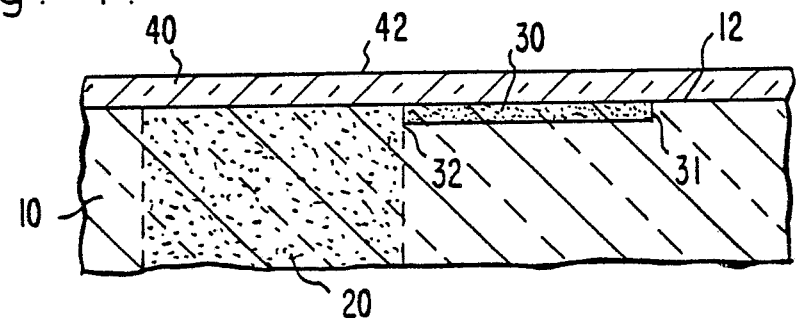
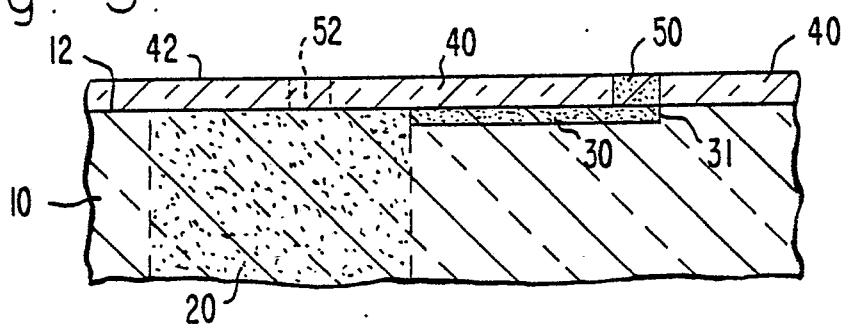


Fig. 5.



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 83/01389

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[3]: H 01 L 23/52; H 01 L 21/74

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC[3]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [6]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US, A, 3787252 (F. FILIPPAZZI, HONEYWELL) 22 January 1974 see figure 1; column 3, line 31 - column 4, line 4 --	1,4,5
A	FR, A, 2295570 (IBM) 16 July 1976 see figure 3c; page 5, line 31 - page 6, line 7 --	1,2,6,7
A	US, A, 3982268 (T. ANTHONY, GENERAL ELECTRIC) 21 September 1976 see figure 1; column 2, lines 51-52 ------	1,3

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
22nd December 1983	23 JAN. 1984
International Searching Authority [1]	Signature of Authorized Officer [20]
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 83/01389 (SA 5818)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 11/01/84

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 3787252	22/01/74	DE-A,C	1933731	12/02/70
		FR-A-	2013735	10/04/70
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