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(54) Title (EN): MEMORY SYSTEM CAPABLE OF REDUCING THE READING TIME

(54) Title (FR): SYSTÈME DE MÉMOIRE CAPABLE DE RÉDUIRE LE TEMPS DE LECTURE

(57) Abstract:

(EN): A bias circuit includes a charging current reproduce unit, a cell current reproduce unit, a current comparator, and a bit line bias generator. The charging current reproduce unit generates a charging reference voltage according to a charging current flowing through a voltage bias transistor. The cell current reproduce unit generates a cell reference voltage according to a cell current flowing through a common source transistor. The current comparator includes a first current generator for generating a replica charging current according to the charging reference voltage, and a second current generator for generating a replica cell current according to the cell reference voltage. The bit line bias generator generates a bit line bias voltage to control a page buffer for charging a bit line according to a difference between the replica charging current and the replica cell current.

(FR): L'invention concerne un circuit de polarisation qui comprend une unité de reproduction de courant de charge, une unité de reproduction de courant de cellule, un comparateur de courant, et un générateur de polarisation de ligne de bits. L'unité de reproduction de courant de charge génère une tension de référence de charge selon un courant de charge circulant à travers un transistor de polarisation de tension. L'unité de reproduction de courant de cellule génère une tension de référence de cellule selon un courant de cellule circulant à travers un transistor de source commune. Le comparateur de courant comprend un premier générateur de courant pour générer un courant de charge de réplique selon la tension de référence de charge, et un second générateur de courant pour générer un courant de cellule de réplique selon la tension de référence de cellule. Le générateur de polarisation de ligne de bits génère une tension de polarisation de ligne de bits afin de commander un tampon de page pour charger une ligne de bits selon une différence entre le courant de charge de réplique et le courant de cellule de réplique.

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