

(12) International Application Status Report

Received at International Bureau: 07 June 2019 (07.06.2019)

Information valid as of: 12 May 2020 (12.05.2020)

Report generated on: 01 October 2020 (01.10.2020)

(10) Publication number:

WO2020/115757

(43) Publication date:

11 June 2020 (11.06.2020)

(26) Publication language:

English (EN)

(21) Application Number:

PCT/IN2019/050437

(22) Filing Date:

07 June 2019 (07.06.2019)

(25) Filing language:

English (EN)

(31) Priority number(s):

201821046452 (IN)

(31) Priority date(s):

07 December 2018 (07.12.2018)

(31) Priority status:

(51) International Patent Classification:

H03L 7/00 (2006.01); **H03H 11/26** (2006.01)

(71) Applicant(s):

VARROC ENGINEERING LIMITED [IN/IN]; L-4, MIDC, Waluj, Maharashtra Aurangabad 431136 (IN) *(for all designated states)*

(72) Inventor(s):

SHARMA, Anupam; Mhalasa Bungalow Lane 4, Veerabhadra Nagar, Baner Pune 411045 Maharashtra (IN)
JALAL, Nafish; House no 449 Deshmukh Moholla Mahad, Raigadh 402301 Maharashtra (IN)

(74) Agent(s):

KHAITAN & CO; One Indiabulls Centre, 13th Floor 841, Senapati Bapat Marg Elphinstone Road Mumbai 400013, Maharashtra (IN)

(54) Title (EN): A CIRCUIT FOR GENERATING A CONTROL VOLTAGE DEPENDING ON VOLTAGE PHASE OF AN INPUT SIGNAL

(54) Title (FR): CIRCUIT POUR GÉNÉRER UNE TENSION DE COMMANDE EN FONCTION DE LA PHASE DE TENSION D'UN SIGNAL D'ENTRÉE

(57) Abstract:

(EN): The present invention provides a circuit for generating a control voltage depending on voltage phase of an input signal. The circuit comprises a first transistor; a second transistor, a diode, a Zener diode and a capacitor. Base and collector of first transistor along with collector of second transistor are connected to a DC voltage source. Anode of the diode is connected to base of the first transistor and cathode of the diode receives the input signal. Anode of the Zener diode is connected to the base of the second transistor and cathode of the Zener diode connected to the collector of the first transistor. The capacitor is connected between cathode of the Zener diode and ground terminal. During positive half cycle and negative half of input signal, the circuit outputs a high control voltage and a low control voltage respectively.

(FR): La présente invention concerne un circuit pour générer une tension de commande en fonction de la phase de tension d'un signal d'entrée. Le circuit comprend un premier transistor, un second transistor, une diode, une diode Zener et un condensateur. La base et le collecteur du premier transistor avec le collecteur du second transistor sont connectés à une source de tension continue. L'anode de la diode est connectée à la base du premier transistor et la cathode de la diode reçoit le signal d'entrée. L'anode de la diode Zener est connectée à la base du second transistor et la cathode de la diode Zener est connectée au collecteur du premier transistor. Le condensateur est connecté entre la cathode de la diode Zener et la borne de terre. Pendant le demi-cycle positif et la moitié négative du signal d'entrée, le circuit délivre une tension de commande élevée et une tension de commande basse respectivement.

International search report:

Received at International Bureau: 29 August 2019 (29.08.2019) [IN]

International Report on Patentability (IPRP) Chapter II of the PCT:

Not available

(81) Designated States:

AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW

European Patent Office (EPO) : AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR

African Intellectual Property Organization (OAPI) : BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG

African Regional Intellectual Property Organization (ARIPO) : BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW

Eurasian Patent Organization (EAPO) : AM, AZ, BY, KG, KZ, RU, TJ, TM

Declarations:

Declaration made as applicant's entitlement, as at the international filing date, to apply for and be granted a patent (Rules 4.17(ii) and 51bis.1(a)(ii)), in a case where the declaration under Rule 4.17(iv) is not appropriate