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(54) Title (EN): FRACTIONAL FREQUENCY SYNTHESIS BY SIGMA-DELTA MODULATING FREQUENCY OF A REFERENCE CLOCK

(54) Title (FR): SYNTHÈSE DE FRÉQUENCE FRACTIONNAIRE PAR LA FRÉQUENCE DE MODULATION SIGMA-DELTA D'UNE HORLOGE DE RÉFÉRENCE

(57) Abstract:
(EN): A circuit (30) includes a programmable frequency divider (14) which receives a high-speed clock (12), fin, as an input and which provides a modulated reference clock (20) as an output; a Sigma-Delta modulator (16) which receives a Frequency Control Word (FCW) (18) and which is connected to the programmable frequency divider (14) to receive the modulated reference clock (20) as a sample clock and to control an average frequency of the modulated reference clock (20); and an integer-N Phase Lock Loop (PLL) (22) which receives the modulated reference clock (20) and outputs a clock output..

(FR): Un circuit (30) comprend un diviseur de fréquence programmable (14) qui reçoit une horloge à grande vitesse (12), fin, en tant qu'entrée et qui fournit une horloge de référence modulée (20) en tant que sortie ; un modulateur Sigma-Delta (16) qui reçoit un mot de commande de fréquence (FCW) (18) et qui est connecté au diviseur de fréquence programmable (14) pour recevoir l'horloge de référence modulée (20) en tant qu'horloge d'échantillon et pour commander une fréquence moyenne de l'horloge de référence modulée (20) ; et une boucle à verrouillage de phase (PLL) à nombre entier N (22) qui reçoit l'horloge de référence modulée (20) et délivre en sortie une sortie d'horloge.

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Declarations:

Declaration made as applicant's entitlement, as at the international filing date, to apply for and be granted a patent (Rules 4.17(ii) and 51bis.1(a)(ii)), in a case where the declaration under Rule 4.17(iv) is not appropriate