# (12) International Application Status Report

**Received at International Bureau:** 28 October 2019 (28.10.2019)
**Information valid as of:** 18 May 2020 (18.05.2020)
**Report generated on:** 20 September 2020 (20.09.2020)

**(10) Publication number:**
WO2020/112259

**(43) Publication date:**
04 June 2020 (04.06.2020)

**(26) Publication language:**
English (EN)

**(21) Application Number:**
PCT/US2019/056029

**(22) Filing Date:**
14 October 2019 (14.10.2019)

**(25) Filing language:**
English (EN)

**(31) Priority number(s):**
16/205,308 (US)

**(31) Priority date(s):**
30 November 2018 (30.11.2018)

**(31) Priority status:**
Priority document received (in compliance with PCT Rule 17.1)

**(51) International Patent Classification:**
***H03L 7/18*** (2006.01); ***H03L 7/22*** (2006.01)

**(71) Applicant(s):**
CIENA CORPORATION [US/US]; 7035 Ridge Road Hanover, MD 21076 (US) *(for all designated states)*

**(72) Inventor(s):**
AOUINI, Sadok; 41 Rue Jean-De La Fontaine Gatineau, QC J9J 2P6 (CA)
MIKKELSEN, Matthew; 1018 Maitland Avenue Ottawa, ON K2C 2B6 (CA)
BEN-HAMIDA, Naim; 67 Abingdon Drive Ottawa, ON K2H 7M5 (CA)
PARVIZI, Mahdi; 308 Glenbrae Avenue Kanata, ON K2W 0B9 (CA)
WEN, Tingjun; 412 Drumheller Place Ottawa, ON K2T 0H2 (CA)
PLETT, Calvin; 12 Confederation Pvt. Ottawa, ON K1V 9W6 (CA)

**(74) Agent(s):**
BARATTA, Lawrence, A., Jr.; Clements Bernard Walker 4500 Cameron Valley Parkway, Suite 350 Charlotte, NC 28211 (US)

**(54) Title (EN):** FRACTIONAL FREQUENCY SYNTHESIS BY SIGMA-DELTA MODULATING FREQUENCY OF A REFERENCE CLOCK

**(54) Title (FR):** SYNTHÈSE DE FRÉQUENCE FRACTIONNAIRE PAR LA FRÉQUENCE DE MODULATION SIGMA-DELTA D'UNE HORLOGE DE RÉFÉRENCE

**(57) Abstract:**
**(EN):** A circuit (30) includes a programmable frequency divider (14) which receives a high-speed clock (12), $fin$, as an input and which provides a modulated reference clock (20) as an output; a Sigma-Delta modulator (16) which receives a Frequency Control Word (FCW) (18) and which is connected to the programmable frequency divider (14) to receive the modulated reference clock (20) as a sample clock and to control an average frequency of the modulated reference clock (20); and an integer-N Phase Lock Loop (PLL) (22) which receives the modulated reference clock (20) and outputs a clock output..

**(FR):** Un circuit (30) comprend un diviseur de fréquence programmable (14) qui reçoit une horloge à grande vitesse (12), $fin$, en tant qu'entrée et qui fournit une horloge de référence modulée (20) en tant que sortie ; un modulateur Sigma-Delta (16) qui reçoit un mot de commande de fréquence (FCW) (18) et qui est connecté au diviseur de fréquence programmable (14) pour recevoir l'horloge de référence modulée (20) en tant qu'horloge d'échantillon et pour commander une fréquence moyenne de l'horloge de référence modulée (20) ; et une boucle à verrouillage de phase (PLL) à nombre entier N (22) qui reçoit l'horloge de référence modulée (20) et délivre en sortie une sortie d'horloge.

**International search report:**
Received at International Bureau: 19 December 2019 (19.12.2019) [EP]

**International Report on Patentability (IPRP) Chapter II of the PCT:**
Not available

**(81) Designated States:**

AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW

European Patent Office (EPO) : AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR

African Intellectual Property Organization (OAPI) : BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG

African Regional Intellectual Property Organization (ARIPO) : BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW

Eurasian Patent Organization (EAPO) : AM, AZ, BY, KG, KZ, RU, TJ, TM

**Declarations:**

Declaration made as applicant's entitlement, as at the international filing date, to apply for and be granted a patent (Rules 4.17(ii) and 51bis.1(a)(ii)), in a case where the declaration under Rule 4.17(iv) is not appropriate