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(54) Title (EN): SYSTEMS AND METHODS FOR DATA PATH POWER SAVINGS IN DDR5 MEMORY DEVICES

(54) Title (FR): SYSTÈMES ET PROCÉDÉS POUR DES ÉCONOMIES D'ÉNERGIE DE CHEMIN DE DONNÉES DANS DES DISPOSITIFS DE MÉMOIRE DDR5

(57) Abstract:

(EN): A memory device includes a data path having a data bus. The memory derive further includes a first one-hot communications interface communicatively coupled to the data bus, and a second one-hot communications interface communicatively coupled to the data bus. The memory device additionally includes at least one memory bank, and an input/output (I/O) interface communicatively coupled to the at least one memory bank via the first one-hot communications interface and the second one-hot communications interface, wherein the first one-hot communications interface is configured to convert a first data pattern received by the I/O interface into one-hot signals transmitted via the data bus to the second one-hot communications interface, and wherein the second one-hot communications interface is configured to convert the one-hot signals into the first data pattern to be stored in the at least one memory bank.

(FR): L'invention concerne un dispositif de mémoire qui comprend un chemin de données comportant un bus de données. Le dispositif de mémoire comprend en outre une première interface de communication 1 parmi n couplée en communication au bus de données, et une seconde interface de communication 1 parmi n couplée en communication au bus de données. Le dispositif de mémoire comprend en outre au moins un bloc mémoire, et une interface d'entrée/sortie (E/S) couplée en communication avec le ou les blocs mémoire par l'intermédiaire de la première interface de communication 1 parmi n et de la seconde interface de communication 1 parmi n, la première interface de communication 1 parmi n étant configurée pour convertir un premier motif de données reçu par l'interface E/S en signaux 1 parmi n transmis par l'intermédiaire du bus de données à la seconde interface de communication 1 parmi n, et la seconde interface de communication 1 parmi n étant configurée pour convertir les signaux 1 parmi n dans le premier motif de données à stocker dans le ou les blocs mémoire.

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Declarations:

Declaration made as applicant's entitlement, as at the international filing date, to apply for and be granted a patent (Rules 4.17(ii) and 51bis.1(a)(ii)), in a case where the declaration under Rule 4.17(iv) is not appropriate

Declaration made as applicant's entitlement, as at the international filing date, to claim the priority of the earlier application, where the applicant is not the applicant who filed the earlier application or where the applicant's name has changed since the filing of the earlier application (Rules 4.17(iii) and 51bis.1(a)(iii))