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(54) Title (EN): LEVEL SHIFTER CIRCUIT AND INTEGRATED CIRCUIT CHIP

(54) Title (FR): CIRCUIT DE DÉCALAGE DE NIVEAU ET PUCE DE CIRCUIT INTÉGRÉ

(54) Title (ZH): 电平移位电路和集成电路芯片

(57) Abstract:

(EN): Provided in the present disclosure are a level shifter circuit and an integrated circuit chip. In said level shifter circuit, access voltage division circuits are additionally arranged between the drain of a P-channel metal oxide semiconductor field effect transistor (PMOS) and the drain of an N-channel metal oxide semiconductor field effect transistor (NMOS), between the source and drain of the PMOS and between the source and drain of the NMOS respectively within a level shifter circuit composed of a first PMOS and a second PMOS that are cross-connected and a first NMOS and a second NMOS that serve as two low voltage domain inversion signal inputs.

(FR): La présente invention concerne un circuit de décalage de niveau et une puce de circuit intégré. Dans ledit circuit de décalage de niveau, des circuits de division de tension d'accès sont agencés de manière complémentaire entre le drain d'un transistor à effet de champ à semi-conducteur à oxyde métallique à canal P (PMOS) et le drain d'un transistor à effet de champ à semi-conducteur à oxyde métallique à canal N (NMOS), entre la source et le drain du PMOS et entre la source et le drain du NMOS respectivement dans un circuit de décalage de niveau composé d'un premier PMOS et d'un second PMOS qui sont connectés en croix et d'un premier NMOS et d'un second NMOS qui servent en tant que deux entrées de signal d'inversion de domaine basse tension.

(ZH): 本公开提供了一种电平移位电路和一种集成电路芯片。在所述电平移位电路中,在由交叉连接的第一P沟道场效应晶体管(PMOS)和第二PMOS以及作为两个低电压域反相信号输入的第一N沟道场效应晶体管(NMOS)和第二NMOS组成的电平移位电路中,在PMOS的漏极和NMOS的漏极之间、PMOS源极和漏极之间和NMOS源极和漏极之间分别增加设置接入分压电路。

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