(12) International Application Status Report

Received at International Bureau: 18 March 2012 (18.03.2012)
Information valid as of: 13 December 2012 (13.12.2012)
Report generated on: 22 January 2020 (22.01.2020)

(10) Publication number:	**(43) Publication date:**	**(26) Publication language:**
WO2013/137860	19 September 2013 (19.09.2013)	English (EN)

(21) Application Number:	**(22) Filing Date:**	**(25) Filing language:**
PCT/US2012/028876	13 March 2012 (13.03.2012)	English (EN)

(51) International Patent Classification:
G06F 1/26 (2006.01); **G06F 1/32** (2006.01); ***G06F 15/80*** (2006.01)

(71) Applicant(s):
INTEL CORPORATION [US/US]; 2200 Mission College Boulevard Santa Clara, California 95052 (US) *(for all designated states except US)*
BHANDARU, Malini K. [US/US]; 52 Surrey Lane Sudbury, Massachusetts 01776 (US) *(for US only)*
DEHAEMER, Eric J. [US/US]; 161 Floral Street Shrewsbury, Massachusetts 01545 (US) *(for US only)*
SHRALL, Jeremy J. [US/US]; 6373 SE Yamhill Street Portland, Oregon 97215 (US) *(for US only)*

(72) Inventor(s):
BHANDARU, Malini K.; 52 Surrey Lane Sudbury, Massachusetts 01776 (US)
DEHAEMER, Eric J.; 161 Floral Street Shrewsbury, Massachusetts 01545 (US)
SHRALL, Jeremy J.; 6373 SE Yamhill Street Portland, Oregon 97215 (US)

(74) Agent(s):
ROZMAN, Mark J.; Trop, Pruner & Hu, P.C. 1616 S. Voss Rd., Ste. 750 Houston, Texas 77057-2631 (US)

(54) Title (EN): DYNAMICALLY COMPUTING AN ELECTRICAL DESIGN POINT (EDP) FOR A MULTICORE PROCESSOR

(54) Title (FR): CALCUL DYNAMIQUE D'UN POINT DE CONCEPTION ÉLECTRIQUE (EDP) POUR UN PROCESSEUR MULTINOYAU

(57) Abstract:
(EN): In one embodiment, a multicore processor includes a controller to dynamically limit a maximum permitted turbo mode frequency of its cores based on a core activity pattern of the cores and power consumption information of a unit power table. In one embodiment, the core activity pattern can indicate, for each core, an activity level and a logic unit state of the corresponding core. Further, the unit power table can be dynamically computed based on a temperature of the processor. Other embodiments are described and claimed.

(FR): Dans un mode de réalisation, un processeur multinoyau comprend un contrôleur pour limiter dynamiquement une fréquence de mode turbo maximum autorisée de ses noyaux sur la base d'un modèle d'activité de noyau des noyaux et d'informations de consommation d'énergie d'une table de puissance d'unité. Dans un mode de réalisation, le modèle d'activité de noyau peut indiquer, pour chaque noyau, un niveau d'activité et un état d'unité logique du noyau correspondant. En outre, la table de puissance d'unité peut être calculée dynamiquement sur la base d'une température du processeur. D'autres modes de réalisation sont décrits et revendiqués.

International search report:
Received at International Bureau: 03 December 2012 (03.12.2012) [KR]

International Report on Patentability (IPRP) Chapter II of the PCT:
Not available

(81) Designated States:

AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW
European Patent Office (EPO) : AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR
African Intellectual Property Organization (OAPI) : BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG
African Regional Intellectual Property Organization (ARIPO) : BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW
Eurasian Patent Organization (EAPO) : AM, AZ, BY, KG, KZ, MD, RU, TJ, TM

Declarations:
Declaration made as to the identity of the inventor (PCT Rules 4.17(i) and 51bis.1(a)(i))