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(54) Title (EN): METHOD AND APPARATUS FOR REDUCING LATENCY ASSOCIATED WITH EXECUTING MULTIPLE INSTRUCTION GROUPS

(54) Title (FR): PROCÉDÉ ET APPAREIL DE RÉDUCTION DE TEMPS D'ATTENTE ASSOCIÉS À L'EXÉCUTION DE GROUPES D'INSTRUCTIONS MULTIPLES

(57) Abstract:
(EN): A method and apparatus for reducing latency in computer processors. The method incorporates a special instruction set that provides an indication of whether a particular instruction is capable of being executed nearly simultaneously with a preceding instruction in the same group. In such a situation, multiple instructions may be executed at a rate faster than expected. A simple apparatus for accomplishing this method is illustrated.

(FR): La présente invention concerne un procédé et un appareil permettant de réduire un temps d'attente dans des processeurs informatiques. Le procédé comprend un ensemble d'instructions particulières qui fournit une indication quant à savoir si une instruction particulière peut être exécutée presque simultanément à une instruction précédente dans le même groupe. Dans une telle situation, plusieurs instructions peuvent être exécutées à une vitesse supérieure à celle prévue. Un simple appareil pour accomplir ce procédé est illustré.

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